INTEGRATED CIRCUITS, SILICON MONOLITHIC,

LOW POWER, QUAD, BIPOLAR OPERATIONAL AMPLIFIERS,

αRD124A

Detail Specification RDm 054

ISSUE 1

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1. GENERAL

1.1 Scope

This specification details the rating, physical and electrical characteristics, test and inspections data for a silicon monolithic, Low Power, Quad, Bipolar Operational Amplifier, based on Types LM124A This document defines screening and conformance inspection requirements and follows the general guidelines of ESCC 9000 for space-level products.

1.2 Maximum Ratings

The maximum ratings, which shall not be exceeded at any time during use or storage, applicable to the integrated circuits specified herein, are as scheduled in Table 2.

1.3 Component Type Variants

Variants of the basic type integrated circuits specified herein, which are also covered by this specification, are given in Table 1.

1.4 Radiation Features

Dose rate = 36 - 360rads(Si)/h

Maximum total dose available RHA designator F 300krads (Si)

1.5 Physical Dimensions

As per Figure 1

1.6 Pin Assignment

As per Figure 2.

1.7 Circuit Schematic

As per Figure 3

1.8 Functional Diagram

As per Figure 4

TABLE 1 - TYPE VARIANTS

Variant	Part	Case	Figure	Package drawing	Weight (gram) no more
01	αRD124A/ABQB	14-lead ceramic flatpack	1	Figure 1	1.50

Notes: AB - Package style (JEP 95, MO-092A, № 14)
Q - Performance grade
B - Ambient operating temperature range (-55ºC,125 ºC)

Table 2 - MAXIMUM RATINGS

No	Characteristics	Symbol	Maximum ratings	Unit	Remarks
1	Supply Voltage	Vcc	32 or ±16	V	-
2	Differential Input Voltage	V_{ID}	32	V	-
3	Input Voltage		−0.3 to +32	V	(1)
4	Input Current (VIN < −0.3V)	I_{IN}	50	mA	(2)
5	Power Dissipation	P_D	700	mW	-
6	Output Short-Circuit Duration (One Amplifier)	Ios(t)	Indefinite		(3)
7	Operating Temperature Range	Top	−55 to +125	°C	-
8	Maximum Junction Temperature	Tj	+150	°C	-
9	Storage Temperature Range	Tstg	−65 to +150	°C	-
10	Lead Temperature (Soldering, 10 seconds)	Tsol	+260	°C	-
11	Thermal conductivity		18	W/mK	
12	ESD Tolerance		250	V	(4)

Notes

(1) For supply voltages less than +32V, the absolute maximum input voltage is equal to supply voltage.

(2) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3VDC (at 25°C).

(3) Short circuits from the output to Vcc can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA, independent of the magnitude of +Vcc. At +Vcc> +15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.

(4) Human body model, 1.5 kΩ in series with 100 pF.

Figure 1 - PHYSICAL DIMENSIONS

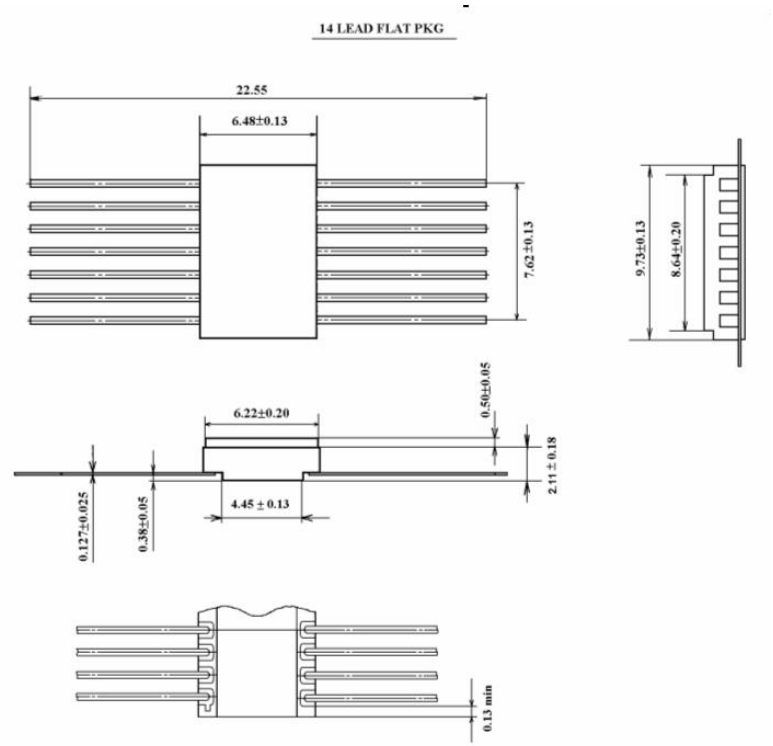


Figure 2 - PIN ASSIGNMENT

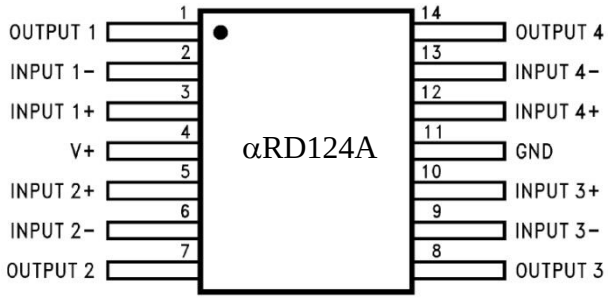


Figure 3 - CIRCUIT SCHEMATIC

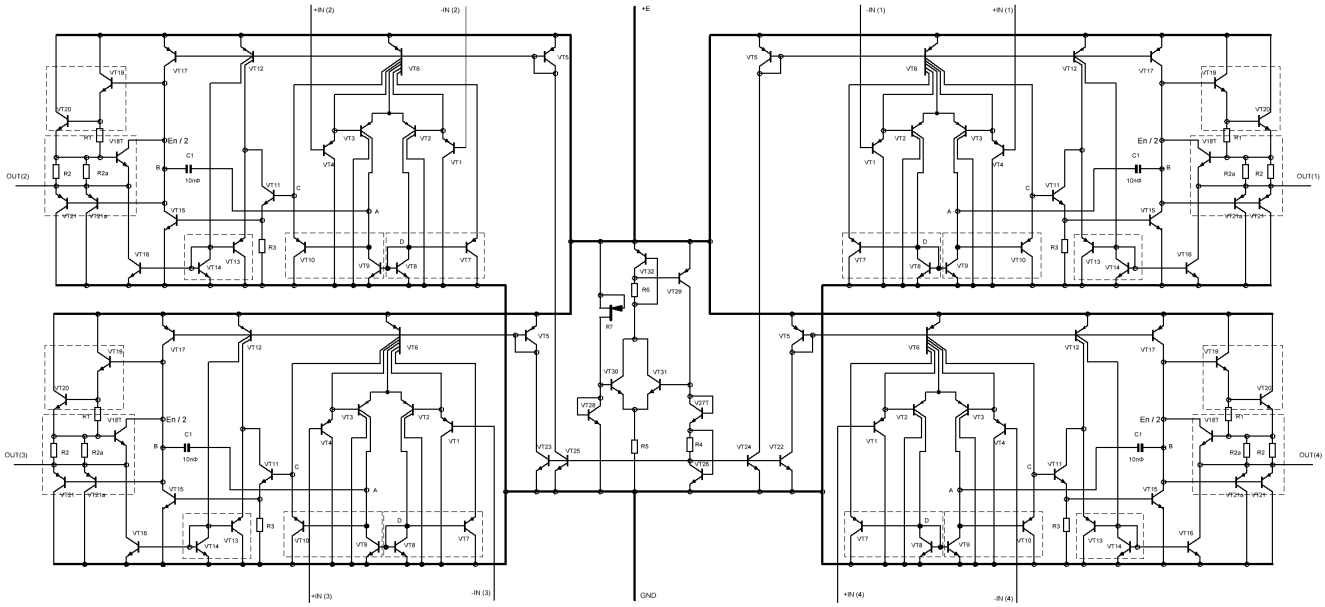
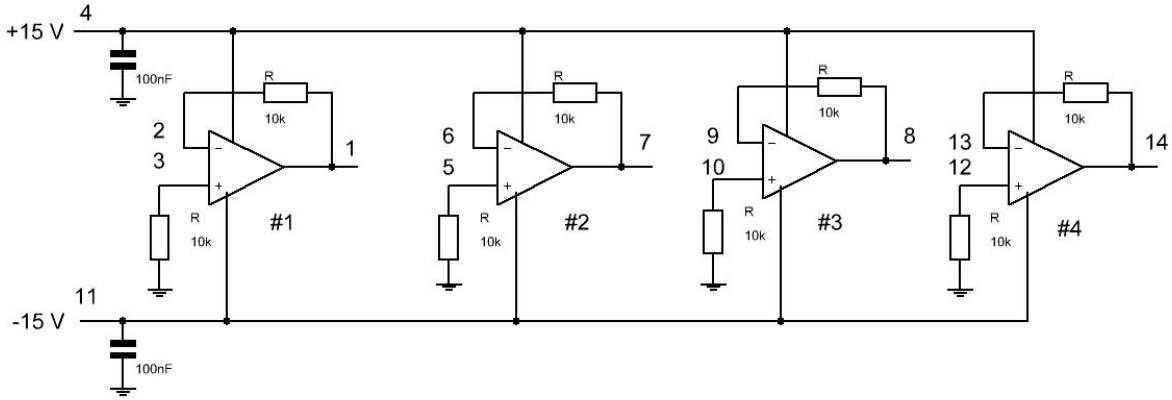


Figure 4 - FUNCTIONAL DIAGRAM



2. APPLICABLE DOCUMENTS

The following documents form part of this specification and shall be read in conjunction with it:

a) ESCC 21300, Terms, Definition, Abbreviation, Symbol And Units
b) ESCC 9000, Integrated Circuits, Monolithic, Hermetically Sealed
c) ESCC 20400, Internal Visual Inspection
d) ESCC 20500, External Visual Inspection
e) ESCC 20600, Preservation, Packaging and Dispatch of ESCC Components
f) ESCC 21700, General Requirements for the Marking of ESCC Components
g) MIL-STD-883, Microcircuit, Test Method Standard

3. TERMS, DEFINITION, ABBREVIATION, SYMBOL AND UNITS

For the purpose of this specification, the terms, definitions, abbreviations, symbols and units specified in ESCC Basic Specification No. 21300 shall apply. In addition, the following abbreviations are used:

Vcc = Supply Voltage of the device under test.
PSRR = Power Supply Rejection Ratio.
OS = Overshoot.
Tr = Rise time.
Rsu = Supply Resistance.
Icc = Supply Current.
Ios(t) = Output Shot Circuit Duration.
TBD = To Be Determined
CSI = Customer Source Inspection
QCI Quality Conformance Inspection

4. REQUIREMENTS

4.1 General

All devices supplied to this specification shall be in accordance with the ESCC 9000 flow requirements, except as specified or modified herein. Single wafer lot and single date code are required.

4.2 Outline Dimension

The dimension of the integrated circuits specified herein shall be checked. They shall conform to those shown in Figure 1. Physical dimensions.

4.2.1 Material and finishes

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the microcircuits specified herein to meet the performance requirements of this specification shall be used. Acceptance or approval of any constituent material does not guarantee acceptance of the finished product.
Pure tin material shall be not used for any internal or external package surface or as a lead finish. Pure tin finish is fully prohibited. Pure tin definition is a percentage of tin superior to 97%.

4.2.2 Case

The case (FP14) shall be hermetically sealed and have ceramic body. The lids shall be welded.

4.2.3 Lead

Lead Finish: gold plate

4.2.4 Marking

The marking of components shall be in accordance with ESCC Basic Specification No. 21700. Laser marking is used, therefore a permanence of markings test (resistance to solvents test as specified in ESCC Basic Specification No. 24800) is not fulfill.

Each component shall be marked in respect of:

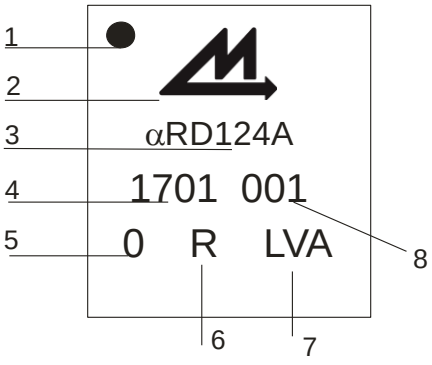


Figure 4a

1. Lead Identification
2. Manufacturer Logo
3. Part number (αRD124A)
4. Lot Date Code
5. ESD Class
6. RHA designator
7. Country of origin
8. Serial Number. The serial number shall be permanently marked on the part for traceability to read and record data.

If device size precludes above marking requirements on the individual part, all of the marking shall be placed on the individual package for each part except that Lead Identification marking, Serial Number, and Lot Date Code, as a minimum, must be placed on the individual devices.

4.2.5 Lead Identification

Key should be located in the upper part of the small lateral plane of the package (Figure 4a, point 1).

4.2.6 Component Number

Each component shall bear the Component Number which shall be constituted and marked as follows:

Detail Specification Number

4.2.7. Traceability Information

Each component should have information about the traceability of production.

4.2.8. Marking of Small Components

The marking information in full shall accompany each component in its primary package

4.3 Electrostatic Discharge Sensitivity

The devices are susceptible to be damaged by electrostatic discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

4.4. Electrical characteristics

4.4.1 Electrical Measurements at Room Temperature

The parameters to be measured in respect of electrical characteristics are scheduled in Table 3(a) and 3(b). Unless otherwise specified, the measurements shall be performed at T_A = +22 ±3 °C.

4.4.2. Electrical Measurements at High and Low Temperatures

The parameters to be measured at high and low temperatures are scheduled in Tables 3(a) and 3(b). The measurements shall be performed at T_A= + 125°C and -55°C respectively.

4.4.3 Circuits for Electrical Measurements

Circuits for use in performing the electrical measurements listed in Tables 2 of this specification are shown in Figure 5.

Table 3(a) - ELECTRICAL MEASUREMENTS DC PARAMETERS (1) (2)

Parameter	Symbol	Test Fg.	Test Method MIL-STD 883	Conditions		T_A, °C	Limits Min	Limits Max	Units
Input Offset Voltage	V_{IO}	7h	4001	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, V_{CM} = +15V		+22 ±3	-2	2	mV
						+125(+0-3)	-4	4	
						-55(+ 5-0)	-4	4	
					R, F	+22 ±3	-2.5	2.5	
				$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_{CM} = -13V		+22 ±3	-2	2	mV
						+125(+0-3)	-4	4	
						-55(+ 5-0)	-4	4	
					R, F	+22 ±3	-2.5	2.5	
				$+V_{CC}$ = 5V, $-V_{CC}$ = Gnd, V_{CM} =+1.4V		+22 ±3	-2	2	mV
						+125(+0-3)	-4	4	
						-55(+ 5-0)	-4	4	
					R, F	+22 ±3	-2.5	2.5	
				$+V_{CC}$ = 2.5V, $-V_{CC}$ = -2.5, V_{CM} = -1.1V		+22 ±3	-2	2	mV
						+125(+0-3)	-4	4	
						-55(+ 5-0)	-4	4	
					R, F	+22 ±3	-2.5	2.5	
Input Offset Current	I_{IO}	7e	4001	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, V_{CM} = +15V		+22 ±3	-10	10	nA
						+125(+0-3)	-10	10	
						-55(+ 5-0)	-30	30	
					R, F	+22 ±3	-15	15	
				$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_{CM} = -13V		+22 ±3	-10	10	nA
						+125(+0-3)	-10	10	
						-55(+ 5-0)	-30	30	
					R, F	+22 ±3	-15	15	
				$+V_{CC}$ = 5V, $-V_{CC}$ = Gnd, V_{CM} = +1.4V		+22 ±3	-10	10	nA
						+125(+0-3)	-10	10	
						-55(+ 5-0)	-30	30	
					R, F	+22 ±3	-15	15	
				$+V_{CC}$ = 2.5V, $-V_{CC}$ = -2.5, V_{CM} = -1.1V		+22 ±3	-10	10	nA
						+125(+0-3)	-10	10	
						-55(+ 5-0)	-30	30	
					R, F	+22 ±3	-15	15	

Table 3(a) - ELECTRICAL MEASUREMENTS DC PARAMETERS (1) (2) (Continued)

Input Bias Current	$\pm I_{IB}$	7e	4001	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, V_{CM} = +15V	+22 ±3	-50	0.1	nA
					+125(+0-3)	-50	0.1	
					-55(+ 5-0)	-100	0.1	
				R	+22 ±3	-75	0.1	
				F	+22 ±3	-130	0.1	
				$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_{CM} = -13V	+22 ±3	-50	0.1	nA
					+125(+0-3)	-50	0.1	
					-55(+ 5-0)	-100	0.1	
				R	+22 ±3	-75	0.1	
				F	+22 ±3	-130	0.1	
				$+V_{CC}$ = 5V, $-V_{CC}$ = Gnd, V_{CM} =+1.4V	+22 ±3	-50	0.1	nA
					+125(+0-3)	-50	0.1	
					-55(+ 5-0)	-100	0.1	
				R	+22 ±3	-75	0.1	
				F	+22 ±3	-130	0.1	
				$+V_{CC}$ = 2.5V, $-V_{CC}$ = -2.5, V_{CM} = -1.1V	+22 ±3	-50	0.1	nA
					+125(+0-3)	-50	0.1	
					-55(+ 5-0)	-100	0.1	
				R	+22 ±3	-75	0.1	
				F	+22 ±3	-130	0.1	
Power Supply Rejection Ratio	+PSRR	7g	4003	$-V_{CC}$ = Gnd, V_{CM} = +1.4V, 5V ≤ V_{CC} ≤ 30V	+ 125°C ÷ -55°C	-100	100	µV/V
Common Mode Rejection Ratio(3)	CMRR	7c	4003	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, V_{CM} = 28.5V	+ 125°C ÷ -55°C	76	-	dB
Short Circiut Output Current	I_{OS}+	7f	3011	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, V_O = 25V	+ 125°C ÷ -55°C	-70	-	mA
Power Supply Current	I_{CC}	7d	4005	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, R_L = 10 kΩ	+22 ±3, +125(+0-3)	-	3	mA
					-55(+ 5-0)	-	4	
				R, F	+22 ±3		3	
Low Level Output Voltage	V_{OL}	7k	3007	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, R_L = 10kΩ	+ 125°C ÷ -55°C	-	35	mV
				R, F	+22 ±3			
				$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, I_{OL} = 5mA	+ 125°C ÷ -55°C	-	1.5	V
				$+V_{CC}$ = 4.5V, $-V_{CC}$ = Gnd, I_{OL} = 2µA	+ 125°C ÷ -55°C	-	0.4	V
High Level Output Voltage	V_{OH}	7j	3006	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, I_{OH} = -10mA	+ 125°C ÷ -55°C	27	-	V
				R, F	+22 ±3			
				$+V_{CC}$ = 4.5V, $-V_{CC}$ = Gnd, I_{OH} = -10mA	+ 125°C ÷ -55°C	2.4	-	V

Table 3(a) - ELECTRICAL MEASUREMENTS DC PARAMETERS (1) (2) (Continued)

Open Loop Voltage Gain (Plus)	+AVS	7a	4004	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, 1V ≤ V_O ≤ 26V, R_L = 10kΩ	+22 ±3	50	-	V/mV
					+125(+0-3), -55(+ 5-0)	25	-	
				R, F	+22 ±3	40	-	
				V_{CC} = 30V, $-V_{CC}$ = Gnd, 5V ≤ V_O ≤ 20V, R_L = 2kΩ	+22 ±3	50	-	V/mV
					+125(+0-3), -55(+ 5-0)	25	-	
				R, F	+22 ±3	40	-	
Open Loop Voltage Gain	AVS	7a	4004	$+V_{CC}$ = 5V, $-V_{CC}$ = Gnd, 1V ≤ V_O ≤ 2.5V, R_L = 10kΩ	+ 125°C ÷ -55°C	10	-	V/mV
				$+V_{CC}$ = 5V, $-V_{CC}$ = Gnd, 1V ≤ V_O ≤ 2.5V, R_L = 2kΩ	+ 125°C ÷ -55°C	10	-	V/mV
Output Voltage Swing (Plus)	V_{OUT} (+)	7b	4004	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, V_O = +30V, R_L = 10kΩ	+ 125°C ÷ -55°C	27	-	V
				$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, V_O = +30V, R_L = 2kΩ	+ 125°C ÷ -55°C	26	-	V
Input Offset Voltage Temperature Sensitivity(4)	$\Delta V_{IO}/\Delta T$	7h	4001	$+V_{CC}$ = 5V, $-V_{CC}$ = 0V, V_{CM} = +1.4V	-55°C ≤ T_A ≤ +25°C	-30	30	µV/ °C
Input Offset Current Temperature Sensitivity(4)	$\Delta I_{IO}/\Delta T$	7e	4001	, $+V_{CC}$ = 5V, $-V_{CC}$ = 0V, V_{CM} = +1.4V	-55°C ≤ T_A ≤ +25°C	-700	700	pA/° C
Input Offset Voltage Temperature Sensitivity(4)	$\Delta V_{IO}/\Delta T$	7h	4001	$+V_{CC}$ = 5V, $-V_{CC}$ = 0V, V_{CM} = +1.4V	+25°C ≤ T_A ≤ +125°C	-30	30	µV/ °C
Input Offset Current Temperature Sensitivity (4)	$\Delta I_{IO}/\Delta T$	7e	4001	, $+V_{CC}$ = 5V, $-V_{CC}$ = 0V, V_{CM} = +1.4V	+25°C ≤ T_A ≤ +125°C	-400	400	pA/° C

Notes:

(1) Post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the line denoted “R” and “F” (correspond to 100 krads (Si) and 300 krads (Si) respectively) of “Conditions” section Table 3(a). These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect.
Radiation end point limits for the noted parameters are ensured only for the conditions as specified in MIL-STD-883, Method 1019

(2) Low dose rate testing should be perform on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

(3) The input common mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is V^+ -1.5 V (at +22 ±3) but either or both inputs can go to +30 V dc without damage independent of the magnitude of V^+

(4) Calculated parameters

Table 3(b) - ELECTRICAL MEASUREMENTS AC PARAMETERS (1) (2)

Parameter	Symbol	Test Fig.	Test Method MIL-STD 883	Test Conditions	T_A, °C	Limits		Units
						Min	Max	
Rise Time	Tr	7l	4002	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd $Vout_{AC}$ = -200mV, $Vout_{DC}$ = +600mV A_{CL}=+1, R_L=2 kΩ, C_L=50pF	+ 125°C ÷ -55°C		1	ms
Overshoot	OS		4002	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd Uout=(0V ÷ + 10V), A_{CL}=+1, R_L=2 kΩ, C_L=50pF	+ 125°C ÷ -55°C		50	%
Slew Rate (Plus)	SR(+)		4002	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, Uout=(0V ÷ + 10V), A_{CL}=+1, R_L=2 kΩ, C_L=50pF	+ 125°C ÷ -55°C	0.1		V/µs
				R, F	+22 ±3			
Slew Rate (Minus)	SR(-)		4002	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, Uout=(0V ÷ +10V), A_{CL}=+1, R_L=2 kΩ, C_L=50pF	+ 125°C ÷ -55°C	0.1		V/µs
				R, F	+22 ±3			
Noise Broadband	NIBB			$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, BW = 10Hz to 5kHz	+22 ±3	-	15	µVrm s
Noise Popcorn	NIPC			$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, R_S = 20kΩ, BW = 10Hz to 5kHz	+22 ±3	-	50	µVpK
Channel Separation (3)	Cs			$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, R_L = 2kΩ	+22 ±3	80	-	dB
				R_L = 2kΩ, V_{IN} = 1V and 16V, A to B		80	-	
				R_L = 2kΩ, V_{IN} = 1V and 16V, A to C		80	-	
				R_L = 2kΩ, V_{IN} = 1V and 16V, A to D		80	-	
				R_L = 2kΩ, V_{IN} = 1V and 16V, B to A		80	-	
				R_L = 2kΩ, V_{IN} = 1V and 16V, B to C		80	-	
				R_L = 2kΩ, V_{IN} = 1V and 16V, B to D		80	-	
				R_L = 2kΩ, V_{IN} = 1V and 16V, C to A		80	-	
Channel Separation (3)	Cs			R_L = 2kΩ, V_{IN} = 1V and 16V, C to B	+22 ±3	80	-	dB
				R_L = 2kΩ, V_{IN} = 1V and 16V, C to D		80	-	
				R_L = 2kΩ, V_{IN} = 1V and 16V, D to A		80	-	
				R_L = 2kΩ, V_{IN} = 1V and 16V, D to B		80	-	
				R_L = 2kΩ, V_{IN} = 1V and 16V, D to C		80	-	

Notes:

(1) Post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the line denoted "R" and "F" (correspond to 100 krads (Si) and 300 krads (Si) respectively) of "Conditions" section Table 3(b). These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect.

Radiation end point limits for the noted parameters are ensured only for the conditions as specified in MIL-STD-883, Method 1019

(2) Low dose rate testing should be perform on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

(3) Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

4.5 Wafer Lot Acceptance

Wafer Lot Acceptance shall be performed in accordance with MIL-STD-883, test method 5007, if specified on the Purchase Order.

4.6 Special In Process Controls

Unless otherwise specified herein, all lots of components used for lot validation testing and for delivery shall be subjected to tests and inspections in accordance with table 4 of this specification.

Any component which do not meet these requirements shall be removed from the lot and no future time be resubmitted to the requirements of this specification.

Table 4 : Special In Process Controls

Component Lot Manufacturing			
Examination or test	**MIL-STD-883 Test Method**	**Test Condition**	**Sample plan**
Internal Visual Inspection	ESCC 20400		100 %
Bond strength (1)	2011	Condition C	2 devices
Die Shear (2)	2019		2 devices
Encapsulation			
Dimension Check	ESCC 20500		2 devices
To Screening tests			

Notes:

(1) Destructive bond pull test

(2) The same test samples submitted to Bond strength

4.7. Burn-In Test

4.7.1. Parameter Drift Value

The parameter drift values applicable to burn-in are specified in Table 5 of this specification. Unless otherwise stated the measurements shall be performed at T_{amb} = (+22±3)°C. The drift values (Δ) applicable to each parameter shall not be exceeded.

Table 5 – PARAMETER DRIFT VALUES FOR BURN-IN TEST AND UPON COMPLETION OF ENDURANCE TESTING

N°	Electrical Parameters	Symbol	Test Conditions	Delta (Δ) Limits		Unit
				Min	Max	
1	Input Offset Voltage	V_{IO}	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, V_{CM} = +15V	-0.5	+0.5	mV
2	Input Bias Current (positive)	$\pm I_{IB}$	$+V_{CC}$ = 30V, $-V_{CC}$ = Gnd, V_{CM} = +15V	-10	0.1	nA

4.7.2. Conditions for Power Burn-In

The requirements for Burn-In are specified in table 6 of this specification. The components shall be subjected to a total power burn-in period of 240 hours.

Table 6 – CONDITIONS FOR POWER BURN IN AND ENDURANCE TEST

N°	Characteristics	Symbol	Condition	Unit
1	Ambient Temperature	T_{amb}	+125	°C
2	Positive supply voltage	V_{CC+}	+16	V
3	Negative supply voltage	V_{CC-}	-16	V
4	Duration	t	240	hours

4.7.3. Electrical Circuit for Power Burn-In

Circuit for use to perform the Power Burn-In tests is shown in Figure 5 of this specification.

FIGURE 5 - POWER BURN-IN AND ENDURANCE TEST ELECTRICAL CIRCUIT

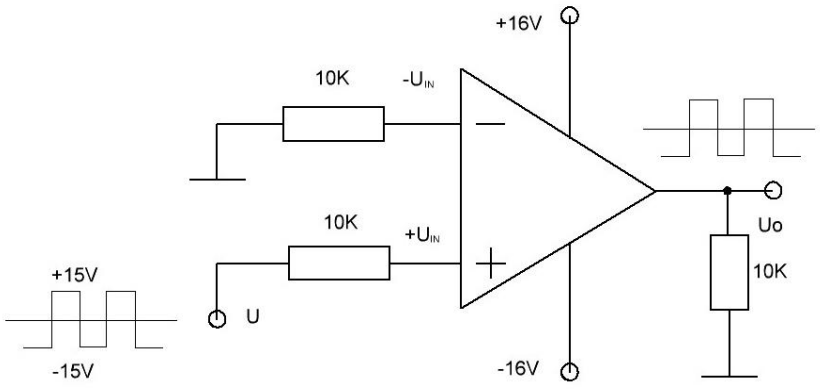


FIGURE 6 - CONNECTION DIAGRAM FOR THE TESTS CONDUCTED UNDER ELECTRICAL LOAD

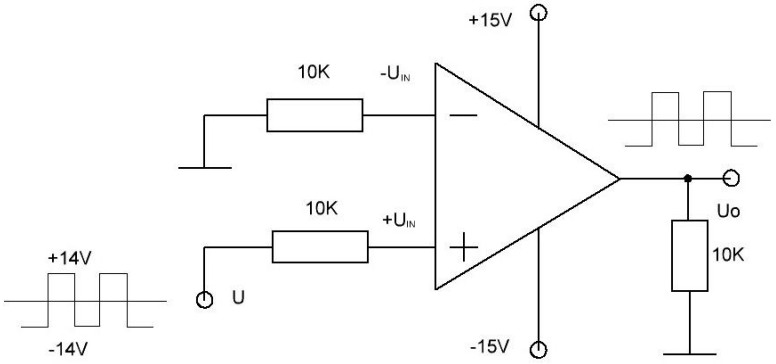
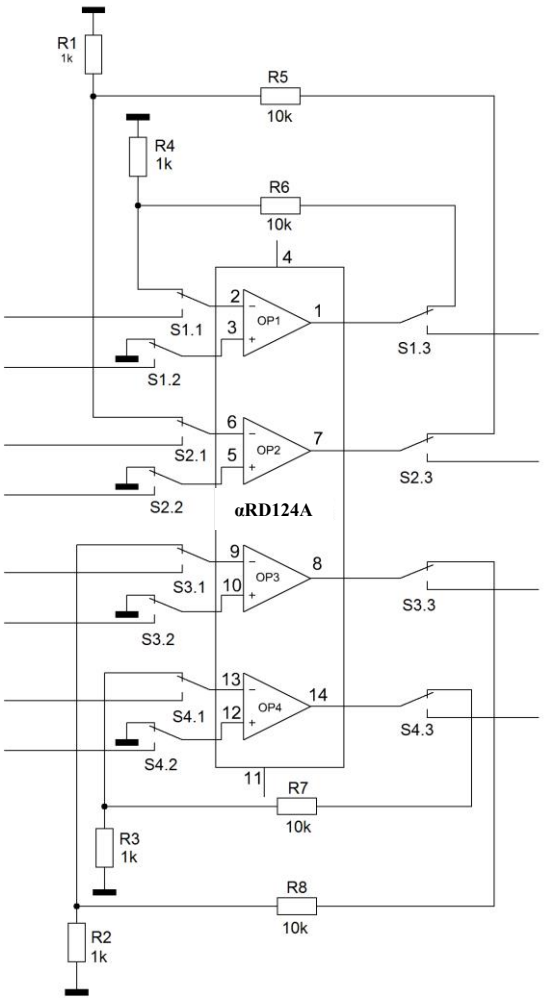


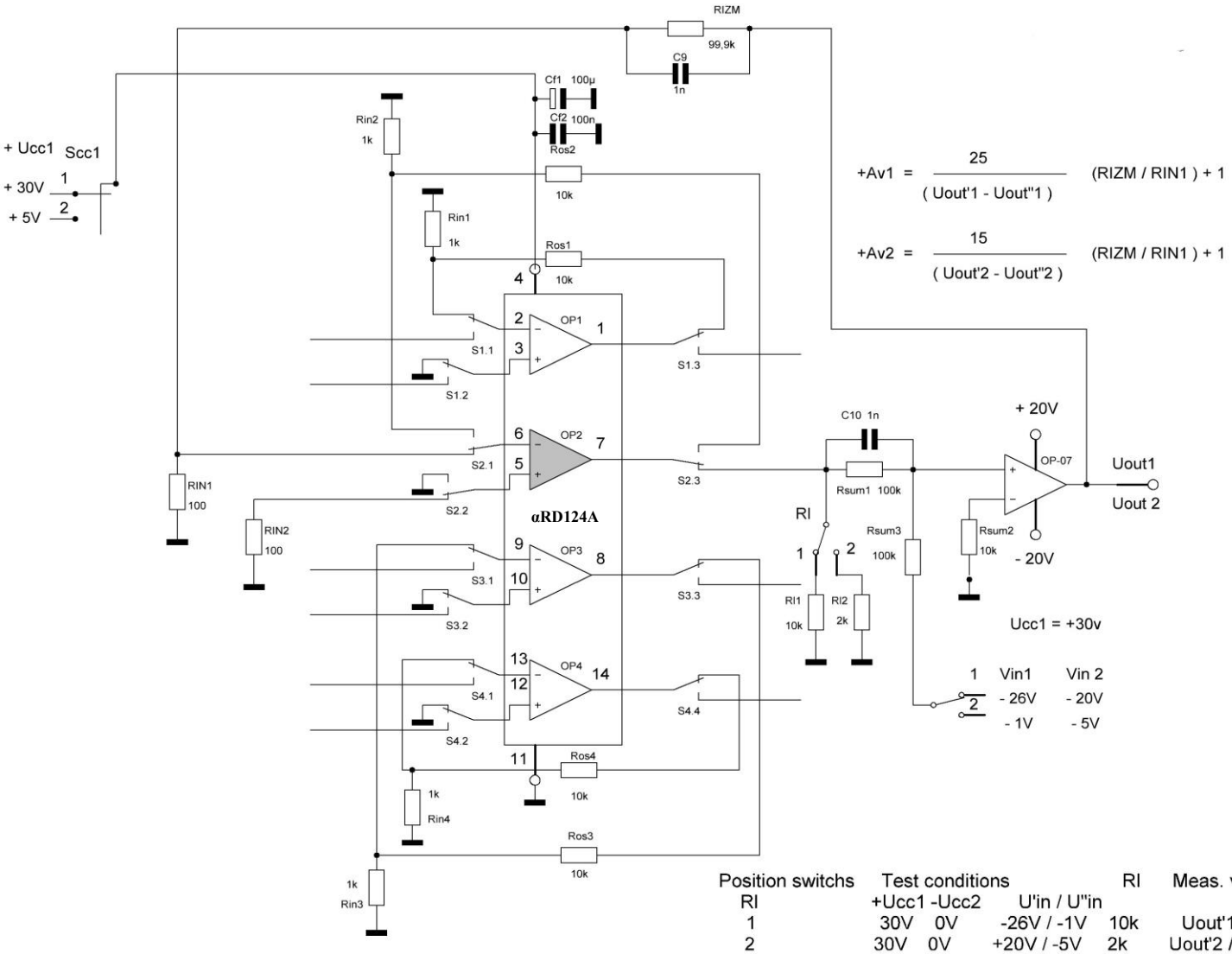
FIGURE 7 – GENERAL CIRCUIT FOR ELECTRICAL MEASUREMENTS DC PARAMETERS



Unused measuring amplifiers are switched in Acl=11

FIGURE 7(a) – OPEN LOOP VOLTAGE GAIN (+30 V)

(Measurements OP2)



Position switchs RI	Test conditions +Ucc1	-Ucc2	U'in / U"in	RI	Meas. value
1	30V	0V	-26V / -1V	10k	Uout'1 / Uout"1
2	30V	0V	+20V / -5V	2k	Uout'2 / Uout"2

FIGURE 7(b) - OPEN LOOP VOLTAGE GAIN (+5 V)

(Measurements OP2)

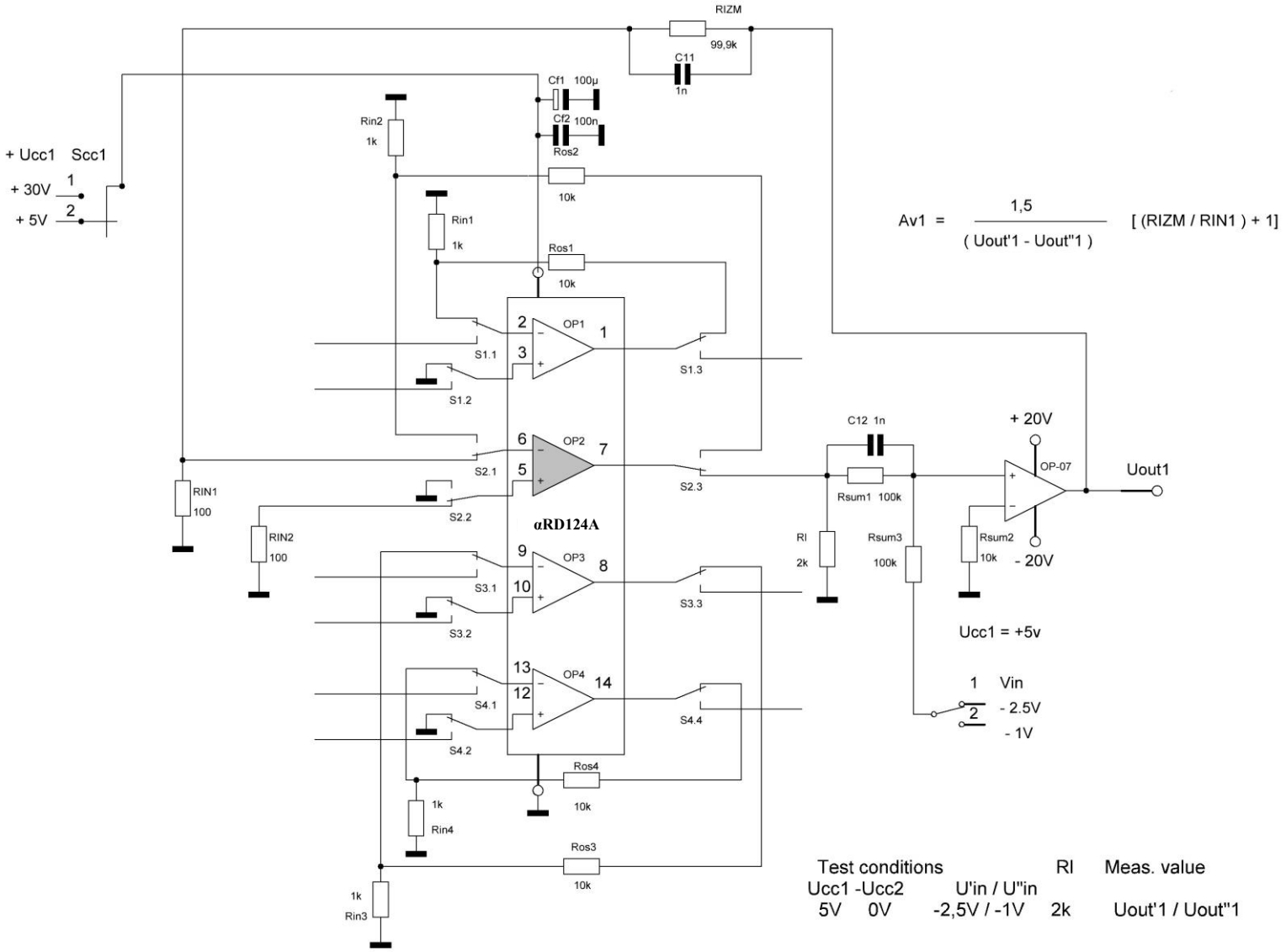
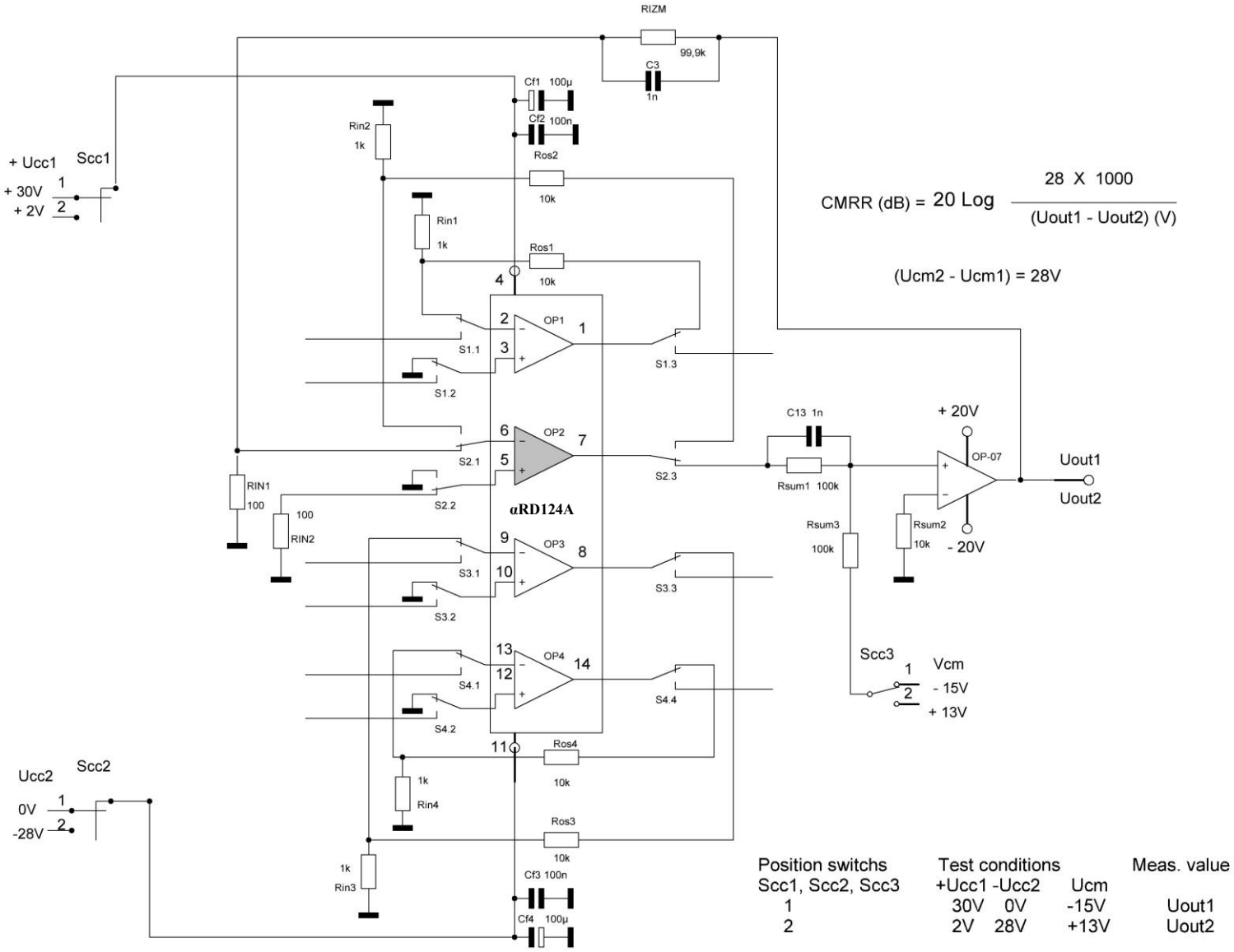


FIGURE 7(c) – COMMON MODE REJECTION RATIO

(Measurements OP2)



Position switchs Scc1, Scc2, Scc3	Test conditions +Ucc1	-Ucc2	Ucm	Meas. value
1	30V	0V	-15V	Uout1
2	2V	28V	+13V	Uout2

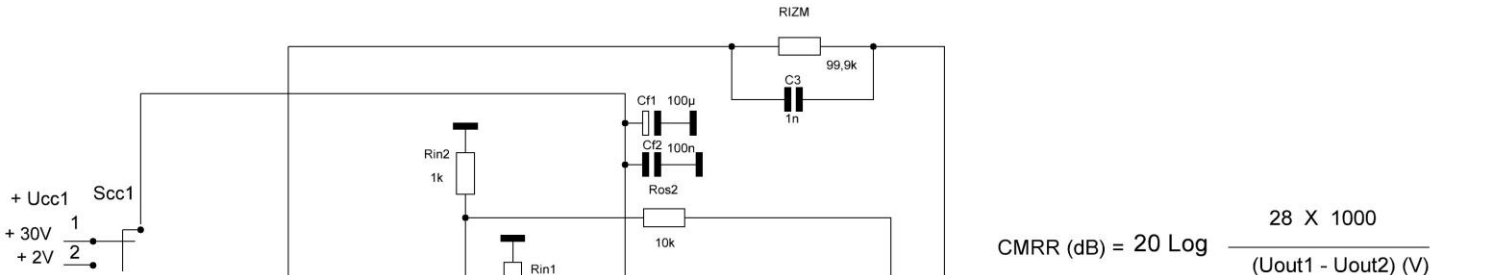


FIGURE 7(d) – POWER SUPPLY CURRENT

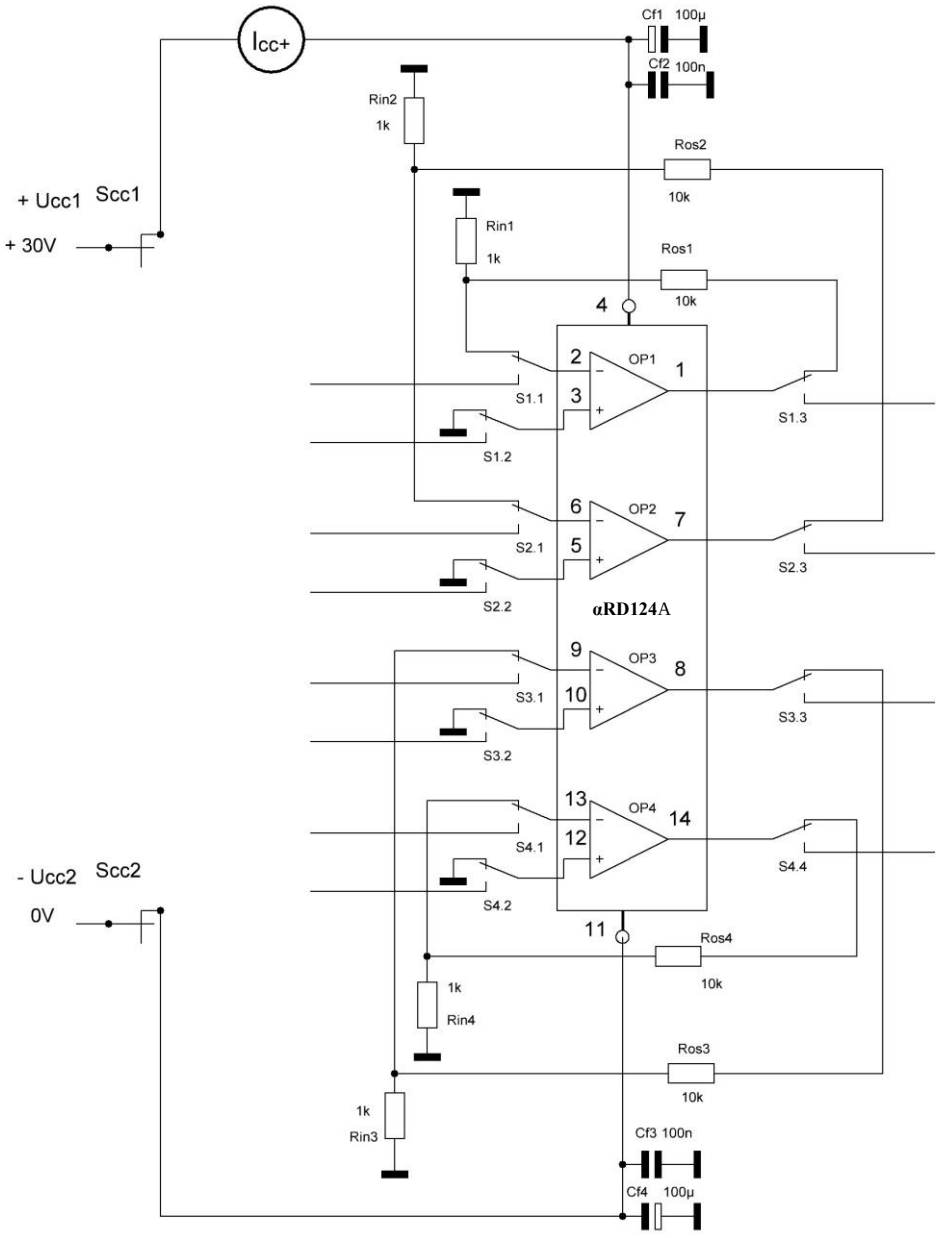
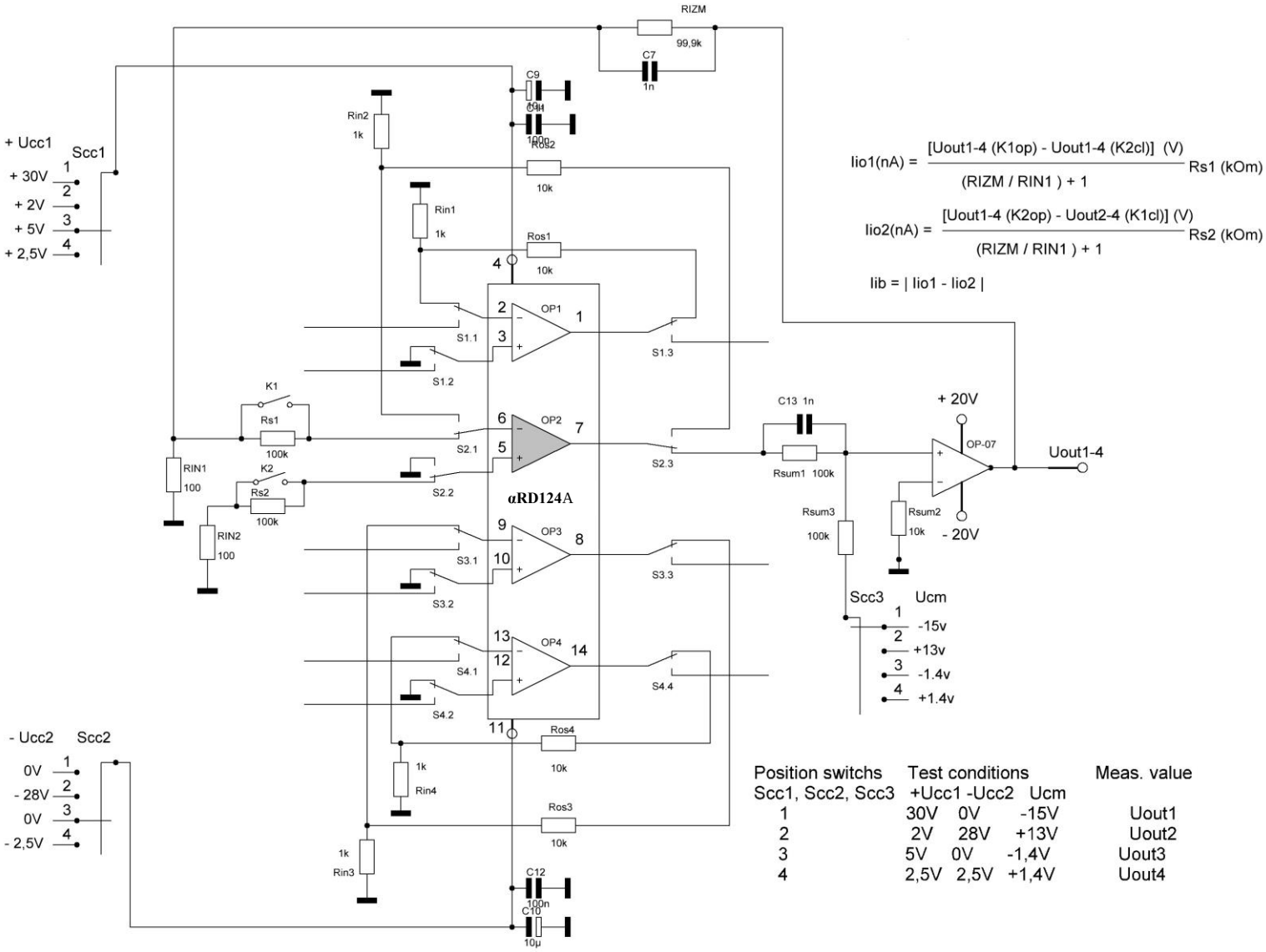


FIGURE 7(e) – INPUT OFFSET AND BAIS CURRENT MEASUREMENTS

(Measurements OP2)



Position switchs Scc1, Scc2, Scc3	Test conditions +Ucc1	-Ucc2	Ucm	Meas. value
1	30V	0V	-15V	Uout1
2	2V	28V	+13V	Uout2
3	5V	0V	-1,4V	Uout3
4	2,5V	2,5V	+1,4V	Uout4

FIGURE 7(f) – SHORT CIRCUIT OUTPUT CURRENT

(Measurements OP2)

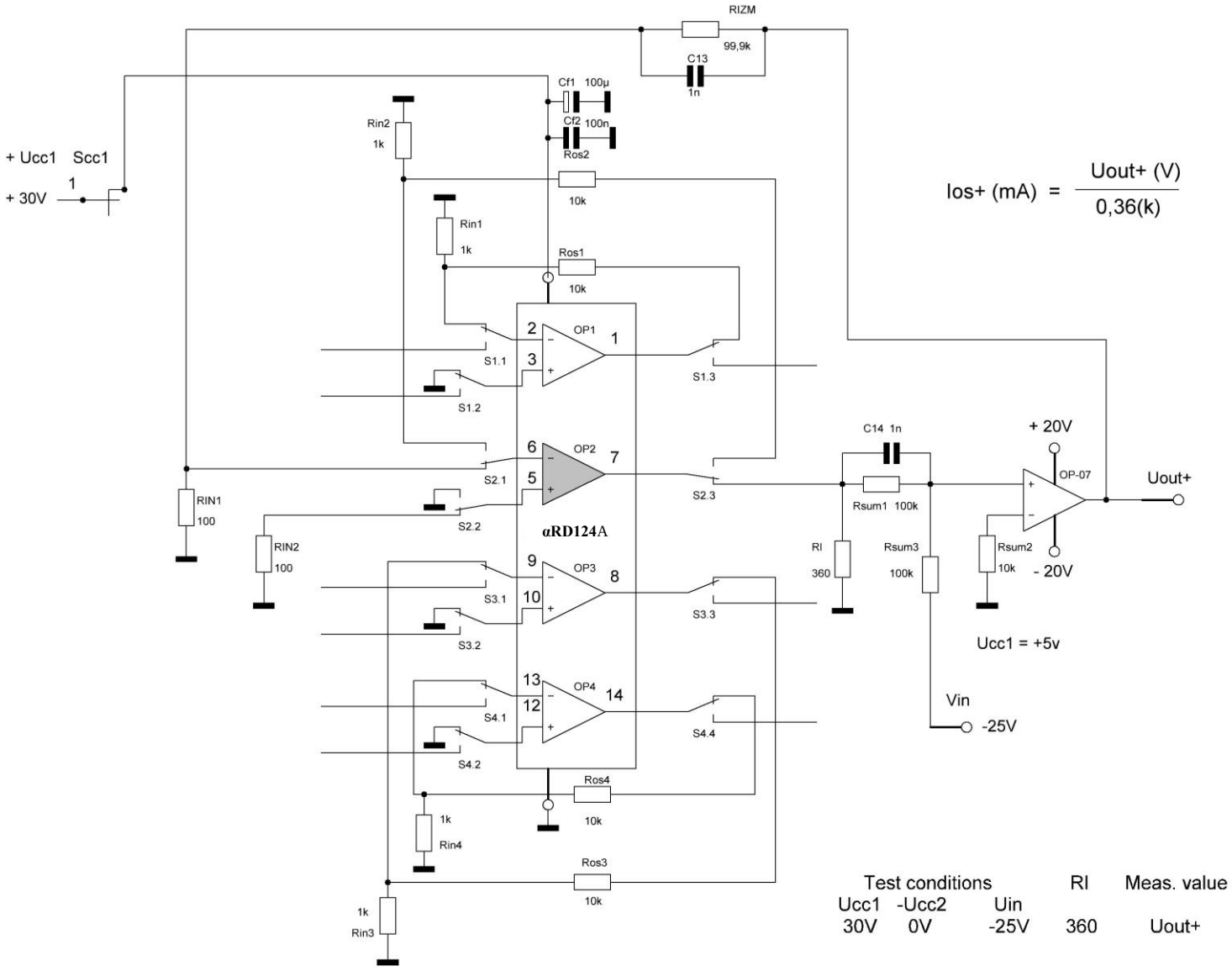
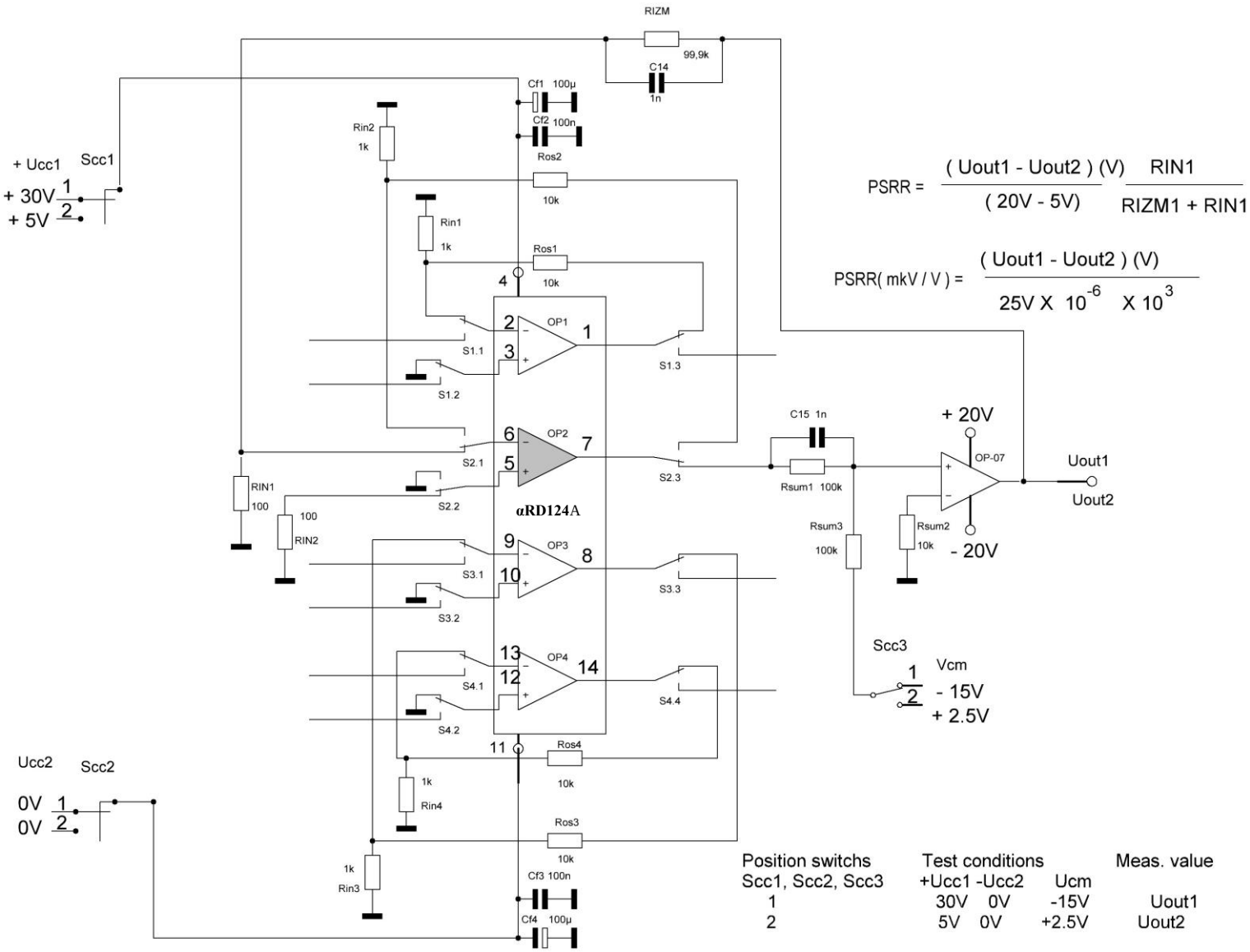


FIGURE 7(g) – POWER SUPPLY REJECTION RATIO

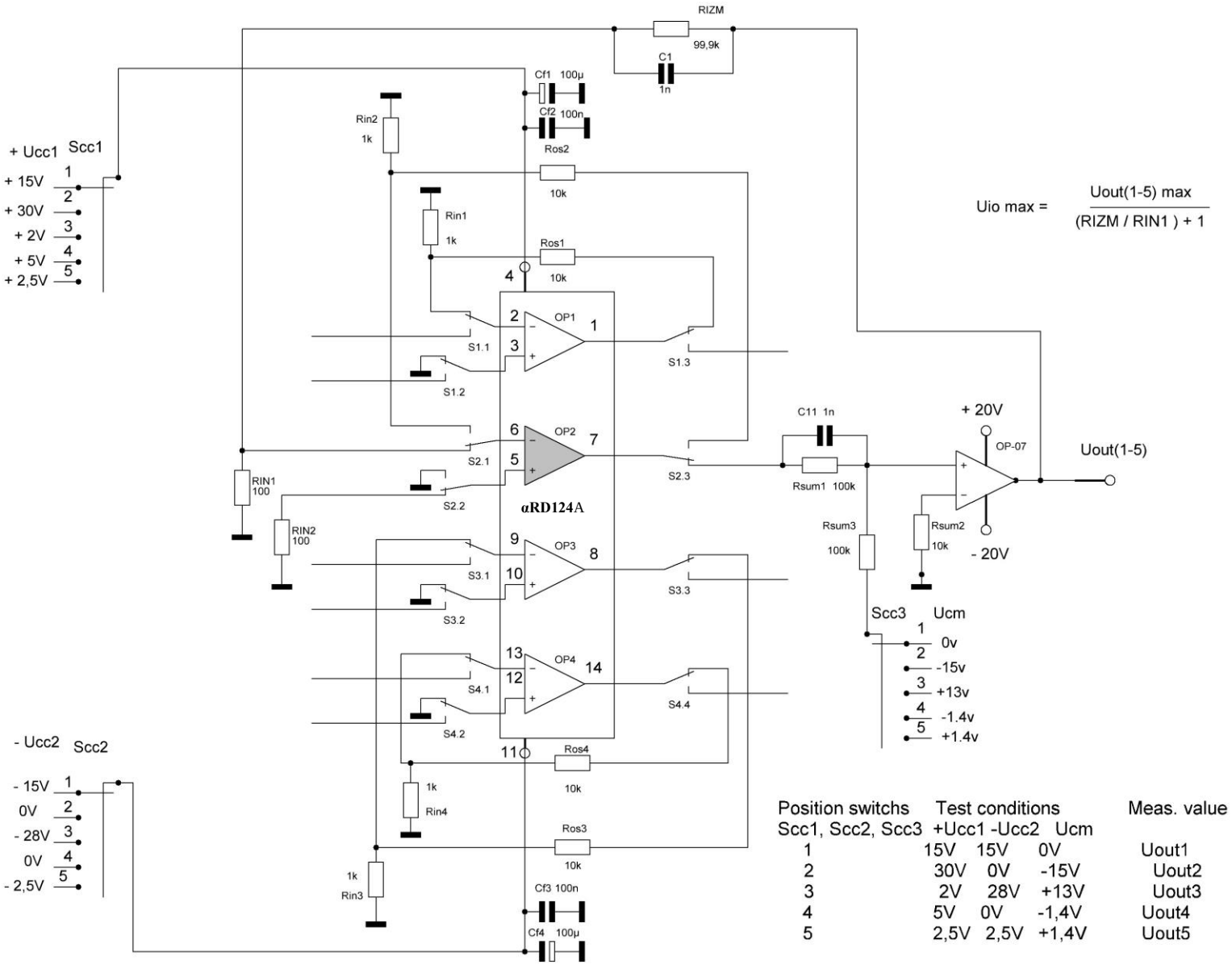
(Measurements OP2)



Position switchs Scc1, Scc2, Scc3	Test conditions +Ucc1	-Ucc2	Ucm	Meas. value
1	30V	0V	-15V	Uout1
2	5V	0V	+2.5V	Uout2

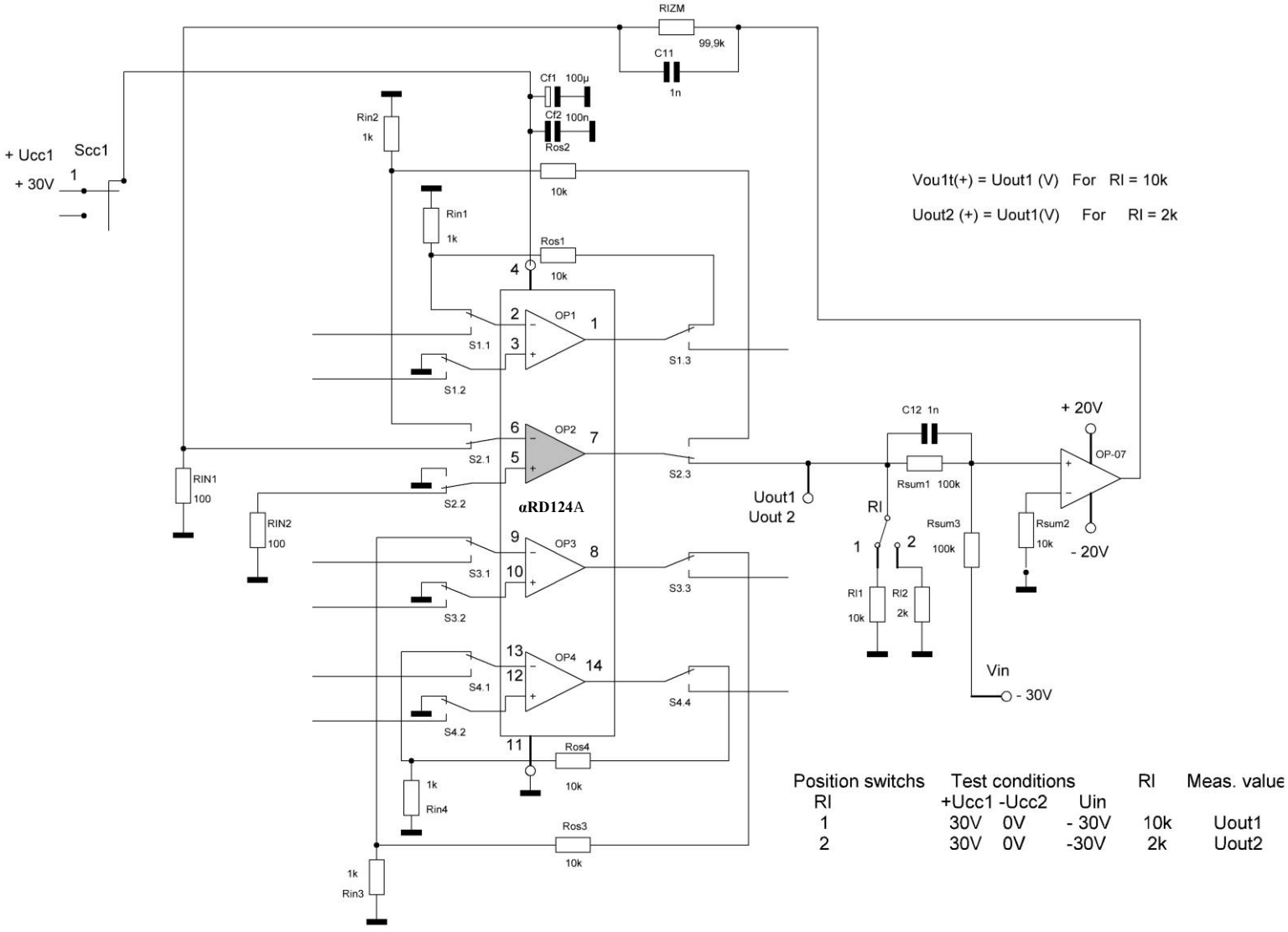
FIGURE 7(h) – INPUT OFFSET VOLTAGE MEASUREMENT

(Measurements OP2)



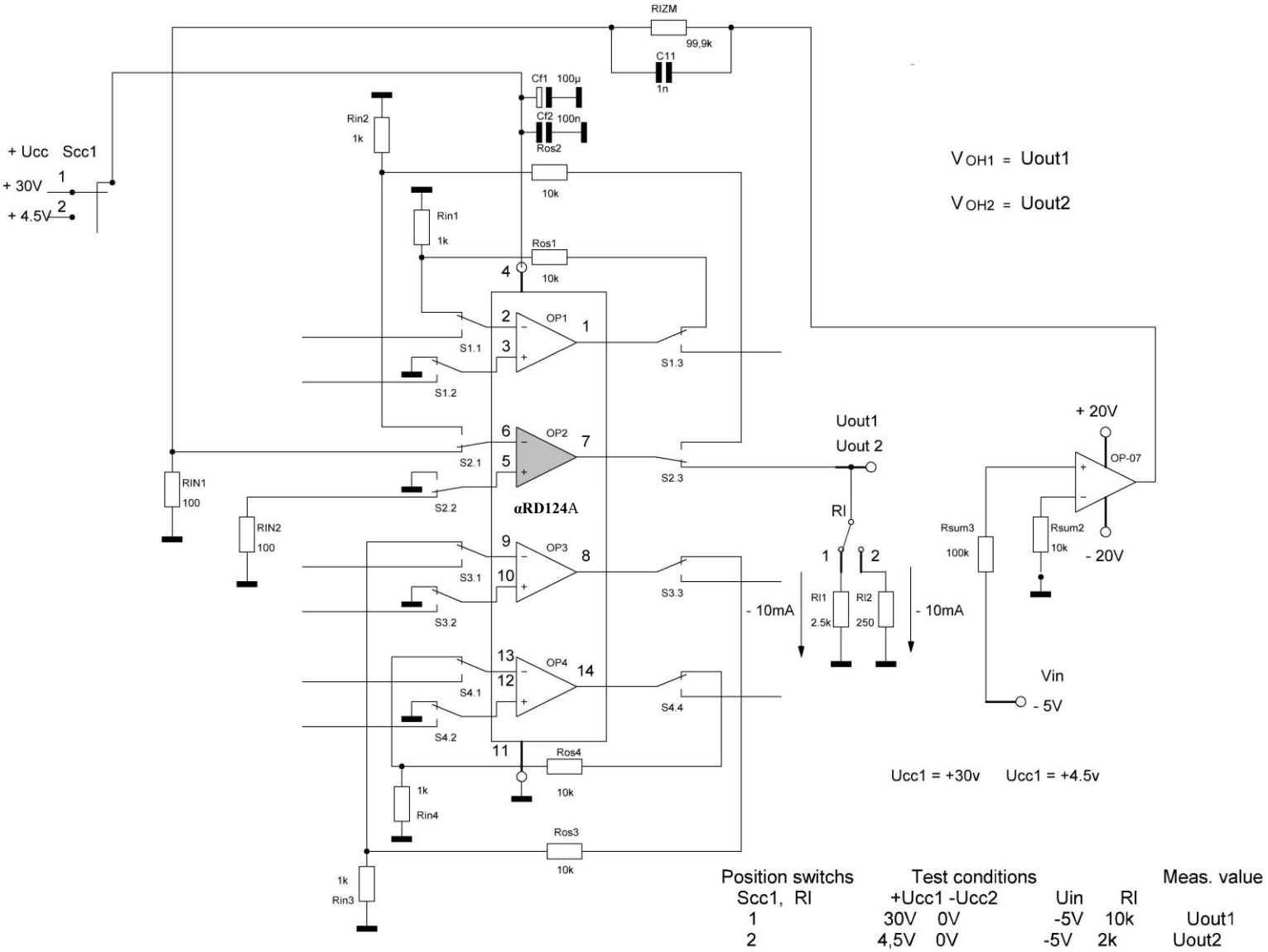
Position switchs Scc1, Scc2, Scc3	Test conditions +Ucc1	-Ucc2	Ucm	Meas. value
1	15V	15V	0V	Uout1
2	30V	0V	-15V	Uout2
3	2V	28V	+13V	Uout3
4	5V	0V	-1,4V	Uout4
5	2,5V	2,5V	+1,4V	Uout5

FIGURE 7(i) – OUTPUT VOLTAGE SWING (PLUS)
(Measurements OP2)



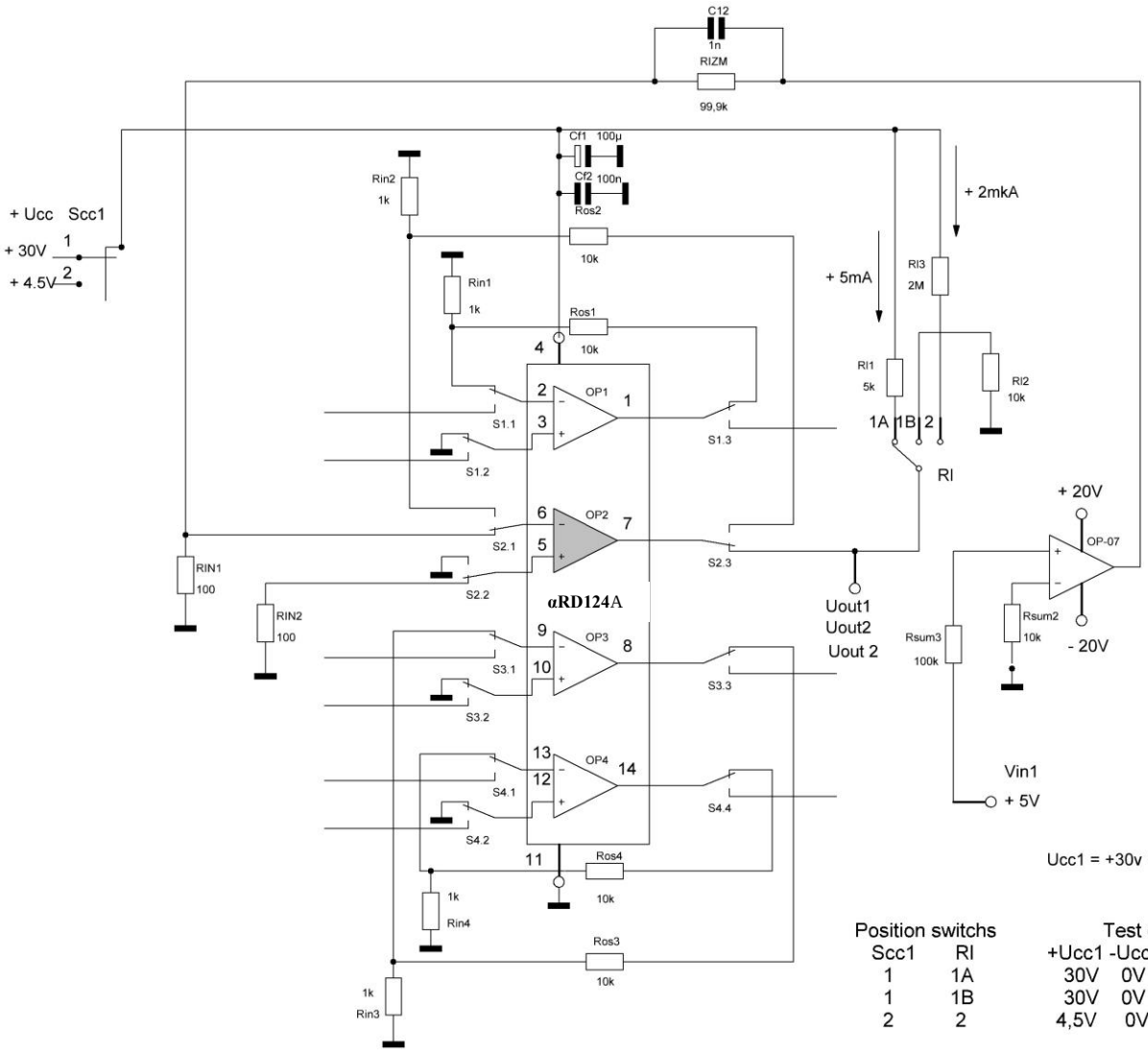
Position switchs RI	Test conditions +Ucc1	-Ucc2	Uin	RI	Meas. value
1	30V	0V	- 30V	10k	Uout1
2	30V	0V	-30V	2k	Uout2

FIGURE 7(j) – OUTPUT VOLTAGE HIGT LEVEL
(Measurements OP2)



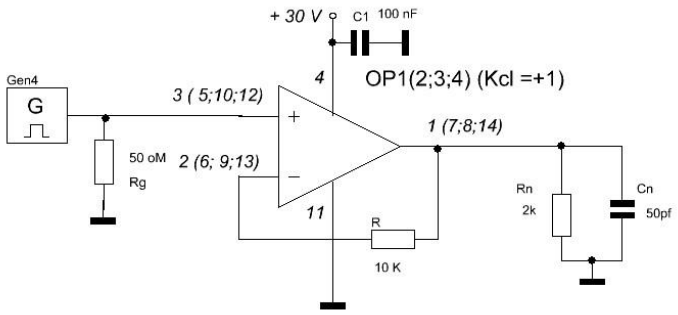
Position switchs Scc1, RI	Test conditions +Ucc1	-Ucc2	Uin	RI	Meas. value
1	30V	0V	-5V	10k	Uout1
2	4,5V	0V	-5V	2k	Uout2

FIGURE 7(k) – OUTPUT VOLTAGE LOW LEVEL
(Measurements OP2)



Position switchs		Test conditions				Meas. value
Scc1	RI	+Ucc1	-Ucc2	Uin	RI	
1	1A	30V	0V	+5V	5k	Uout1
1	1B	30V	0V	+5V	10k	Uout2
2	2	4,5V	0V	+5V	2M	Uout3

FIGURE 8 – DYNAMIC TEST MEASUREMENT CIRCUIT



NOTES:

1. Pulse Generator: rise time ≤ 50 ns, repetition rate 1.0 kHz (max).
2. All resistors are ± 0.1% tolerance and capacitors are ±10% tolerance.

FIGURE 8(a) **SLEW RATE WAVEFORMS**

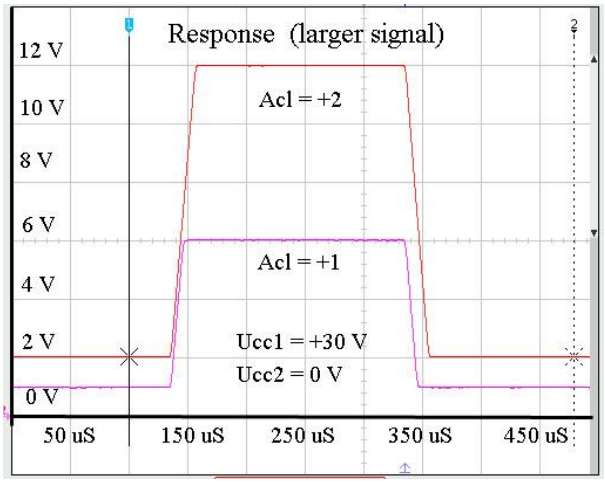
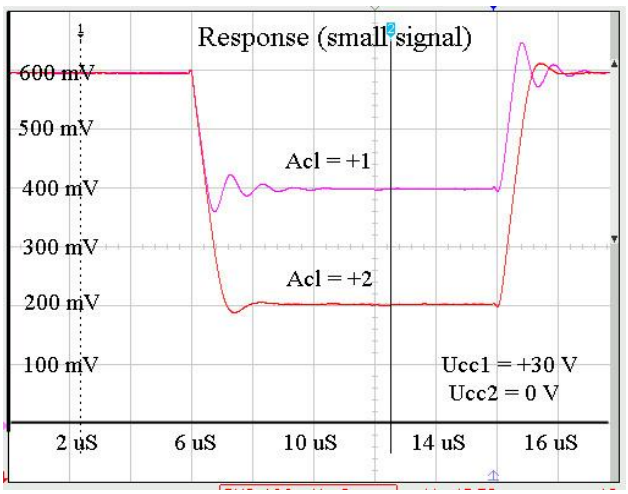


FIGURE 8(b) **OVERSHOOT AND RISE TIME WAVEFORMS**



5 QUALITY ASSURANCE PROVISIONS

5.1 General

The inspection, general procedures for acceptance, and inspection conditions and methods of testing shall be in accordance with this specification, seller quotation, and buyer purchase order.

5.2 Quality Control practices

The manufacturer shall establish and maintain a quality control inspection system in accordance with ESCC 9000, chapter 7, requirements. The manufacturer shall notify the procuring activity of any changes to its drawings and process specifications that affect form, fit, function, or reliability of this part

5.3 Test Equipment and Inspection Facilities

Test and measuring equipment and inspection facilities of sufficient accuracy, quality, and quantity to permit performance of the required inspection shall be established and maintained by the supplier.

5.4 Inspection

The manufacturer is responsible for the performance of all inspection requirements as specified herein and shall provide a certificate of compliance and summary of parts fallout with each item furnished in accordance with this document.

5.4.1 Precap CSI Inspection

Precap CSI inspection shall be performed after manufacturer's precap inspection, if specified on the Purchase Order.

5.4.2 Quality Conformance Inspection: QCI (Final Acceptance Inspection)

Final CSI inspection shall be specified on the Purchase Order, if required.

5.5 Screening Requirements

Each device shall be screened in accordance with ESCC 9000 requirements and as specified in table 7.

Table 7 – SCREENING REQUIREMENTS

Item	Screen	MIL-STD-883 Test Method	Detail and Conditions T_{amb} = 22±3°C unless otherwise specified
1	Precap – Internal Visual		ESCC Basic Specification No. 20400
2	Serialization		
3	High Temperature Stabilization Bake	1008	Duration 24 hours at maximum storage temperature rating
4	Temperature cycling	1010	Condition C ; -65°C to 150°C, 10 cycles, 10 minutes min at each extreme
5	Particle Impact Noise Detection (PIND)	2020	Condition A
6	Radiography	2012	2 views
7	Initial electrical measurements – Ambient temperature		As per tables 3(a), 3(b)
8	Electrical measurements High and Low temperature (go-no go)		As per tables 3a, 3b
9	Power Burn-In	1015	Condition B ; t = 240 hours ; Tamb = 125°C.
10	Final electrical measurements - Ambient temperature		Repeat Initial measurements as per tables 3(a), 3(b). Measurements shall be made within 96 hours of bias removal - Read and record required
11	Final electrical measurements High and Low temperature		As per tables 3(a), 3(b).
12	Check for lot failure - PDA calculation		PDA_{max} = 5 %
13	Hermetic seal Fine and Gross leak	1014	Test condition A (fine leak) Test condition C (gross leak)
14	External Visual Inspection and dimension check		ESCC Basic Specification No. 20500
15	Hot solder dip (if applicable)		

5.5.1 Percent Defective Allowable (PDA)

PDA over Burn-In is 5%. PDA calculation shall include room temperature electrical measurements, high and low temperature electrical measurements and drift calculations.

5.6 Quality Conformance Inspection : QCI (Final Acceptance Inspection)

5.6.1 Environmental / Mechanical Subgroup

Environmental / Mechanical subgroup tests have to be done in accordance with ESCC 9000 chart F4A and table 8 here-in. No reject shall be allowed.

This test is optional and has to be defined / written in the purchase order.

Table 8 : ENVIRONMENTAL / MECHANICAL SUBGROUP TESTS

Examination or test	MIL-STD-883 Test Method	Test Condition	Sample plan
Mechanical Subgroup			
Mechanical shock	2002	Condition B	15 devices
Vibration	2007	Condition A	15 devices
Constant acceleration	2001	Condition E	15 devices
Hermetic seal Fine and Gross leak	1014	Test condition A (fine leak) Test condition C (gross leak)	15 devices
Intermediate and end-point electrical measurements		As per table 3(a)	15 devices
External visual inspection	ESCC Basic Specification No. 20500		15 devices
Environmental Subgroup			
Temperature Cycling	1010	Condition C	15 devices
Moisture resistance	1004		15 devices
Hermetic seal Fine and Gross leak	1014	Test condition A (fine leak) Test condition C (gross leak)	15 devices
Intermediate and end-point electrical measurements		As per table 3(a)	15 devices
External visual inspection	ESCC Basic Specification No. 20500		15 devices

5.6.2 Endurance Capability Subgroup

Endurance subgroup tests have to be done in accordance with ESCC 9000 chart F4A and table 9 here-in. No reject shall be allowed.

Endurance subgroup test is required for the first procurement and must be done again if :

- integrated circuit dice are from a different diffusion lot
- last endurance subgroup exceeds two years of last received Date Code

Table 9 : ENDURANCE CAPABILITY SUBGROUP TESTS

Examination or test	MIL-STD-883 Test Method	Test Condition	Sample plan
Operating life 2000 hours	1005	As per table 6	15 devices
Intermediate and end-point electrical measurements		As per table 3(a)	15 devices
Hermetic seal Fine and Gross leak	1014	Test condition A (fine leak) Test condition C (gross leak)	15 devices
External visual inspection	ESCC Basic Specification No. 20500		15 devices

5.6.3 Assembly Capability Subgroup

Assembly capability subgroup tests shall be conducted in accordance with ESCC 9000 chart F4A and table 10 here-in. No reject shall be allowed.

This test is not optional and shall be ordered in every purchase order.

Table 10 : ASSEMBLY CAPABILITY SUBGROUP TESTS

Examination or test	MIL-STD-883 Test Method	Test Condition	Sample plan
Permanence of marking	ESCC Basic Specification N° 24800		(N/A due to laser marking)
Terminal strength	2004	Condition B2, 3 leads (excluding corner leads) or 10 % of the leads (whichever is greater) shall be randomly selected on each component.	5 devices
Internal visual inspection	ESCC Basic Specification N° 20400		5 devices
Bond strength	2011	Condition C	5 devices
Die shear	2019		5 devices

6. DOCUMENTATION

The manufacturer shall submit the following documentation with each shipment :

- Certificate of Conformance (See chapter 7)
- Serial number Log Sheet
- Summary report (attribute data) of screening process and results (variable data).
- Burn-In Electrical test data and Delta calculations
- Copy of screening

7. CERTIFICATE OF CONFORMANCE

The certificate of conformance consists of and includes as a minimum :

- RD Alfa Part Number
- Rd Alfa sales order
- Date code
- Assembly Lot
- Diffusion Lot
- Dice identification (mask reference)
- ESD HBM Class
- Assembly & Screening manufacturing location
- Detail specification with the applicable revisions
- Shipped quantity

  Serial Numbers

8. PREPARATION FOR DELIVERY

8.1 PACKING AND PACKAGING

The device shall be packaged to prevent mechanical damage in accordance with ESCC 20600. The packing is TBD.

8.1.1 Protection Against Electrostatic Discharge

Each device shall be packaged in a static dissipative static shielded waffle pack to prevent ESD damage according to ESD HBM class in Certificate of Conformance.

8.1.2 Package Identification

Package label shall contain, as a minimum, the following:

- Part number
- Date code
- Purchase order number
- ESD Label.

9. Data reporting

9.1 COVERSHEET

The coversheet of the documentation shall state:

- Applicable specifications references,
- References of the order(s),
- Part number and type designation,
- Manufacturing date
- Lot identification,
- Range of serial numbers (when serialization required) separated for deliverable parts and for parts used for lot acceptance test (qualification),
- Manufacturer name and address,
- Information on deviations,
- Certificate of conformance
- Date and signature of manufacturer

9.2 SUMMARIES

The documentation shall contain separate summaries for:

- Lot traceability certification of compliance
- Final production test, screening and qualification

The minimum statement per summary shall be as follows:

- Test or measurement number,
- Number of "good" parts before test,
- Number of "good" parts after test,
- Failed parts serial number,
- Final results,

- Radiographs (when applicable)
- SEM report

9.3 REJECT LIST

THE DOCUMENT SHALL CONTAIN A REJECT LIST WITH:

- Test or measurement number,
- Serial number of failed parts, failed parameters, failure mode.

9.4 DATA RECORDS

For ESCC screening and lot qualification, complete data records are required, with indication for each part of:

- Serial number part,
- Test or measurement number

Revision History

Date	Release	Used Documents	Changes	Originator