Silicon Monolithic, Low Power, Low Offset Quad, Bipolar Voltage Comparator

Integrated Circuits αRD139A

General Description

The **αRD139A** series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage. Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The **αRD139A** series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the **αRD139A** is a distinct advantage over standard comparators.

The **αRD139A** device is characterized for operation over the full temperature range of –55°C to +125°C.

Features

- **Available with Radiation Ensured:**
  - **Total Ionizing Dose 100 krad(Si), dose rate = 36 - 360rads(Si)/h**
  - **No SEDR was observed with a LET of 62.5 MeV.cm²/mg, Xenon heavy ion.**
  - **Single event transient (SET): σ_{sat}<1.0E-3 cm² at LET= 62.5 MeV·cm²/mg, LET_{th}> 5.7 MeV·cm²/mg.**
- **Wide Supply Voltage Range αRD139A: 2 to 36 V_{DC} or ±1 to ±18 V_{DC}**
- **Very Low Supply Current Drain (0.8 mA) (Typical) — Independent of Supply Voltage**
- **Low Input Biasing Current: 25 nA (Typical)**
- **Low Input Offset Current: ±5 nA (Typical)**
- **Offset Voltage: ±1 mV (Typical)**
- **Input Common-mode Voltage Range Includes GND**
- **Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage: ±36 V**
- **Low Output Saturation Voltage: 250 mV at 4 mA (Typical)**
- **Output Voltage Compatible with TTL, DTL, ECL, MOS and CMOS Logic Systems**

Advantages

- High Precision Comparators
- Reduced V_{OS} Drift Over Temperature
- Eliminates Need for Dual Supplies
- Allows Sensing Near GND
- Compatible with all Forms of Logic
- Power Drain Suitable for Battery Operation

Ordering information

Table 1

Part	Temp. range, °C	Package	Package drawing	Burn-In case temp, °C	Burn-In time, hrs
αRD139A	–55 to +125	14-lead ceramic flatpack	Figure 3	+125	240

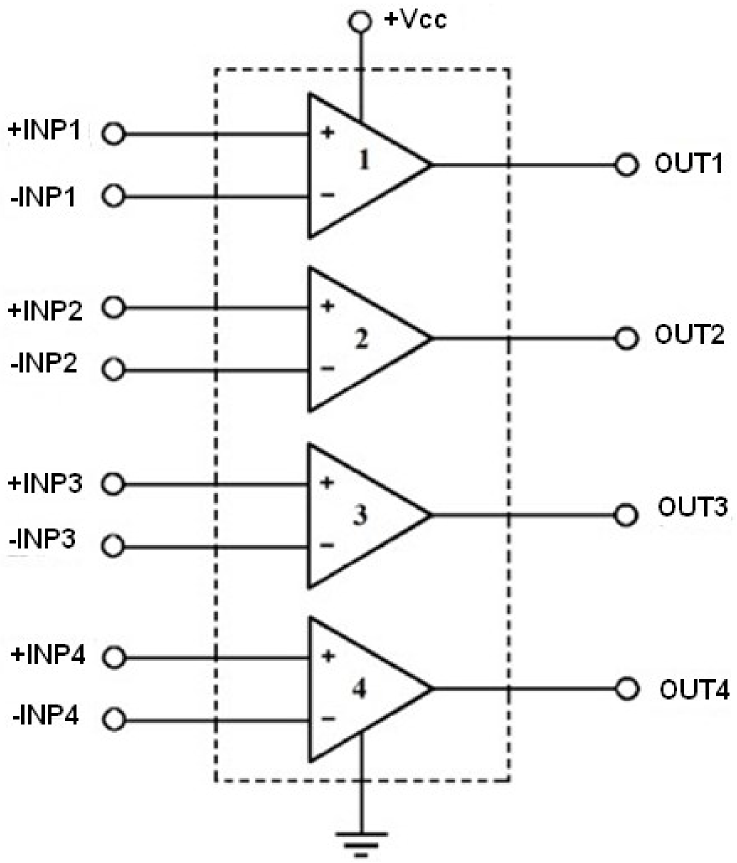
Pin Function Description

Table 2

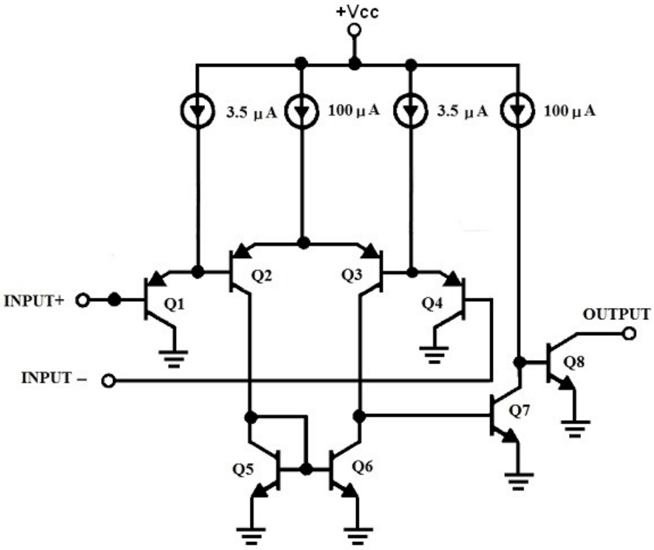
Description	Mnemonic	Pin No
Output 2	OUT 2	1 (Mark)
Output 1	OUT 1	2
Positive Supply	Vcc	3
Negative Input 1	-IN 1	4
Positive Input 1	+IN 1	5
Negative Input 2	-IN 2	6
Positive Input 2	+IN 2	7
Negative Input 3	-IN 3	8
Positive Input 3	+IN 3	9
Negative Input 4	-IN 4	10
Positive Input 4	+IN 4	11
GND (-Vcc)	GND (-Vcc)	12
Output 4	OUT 4	13
Output 3	OUT 3	14

Functional Diagram

Figure 1



Circuit Schematic



Repeated 4 times

Absolute maximum ratings

Table 3

No.	CHARACTERISTICS	SYMBOL	MAXIMUM RATINGS	REMARKS
1	Supply Voltage	Vcc	36 V or ±18 V	
2	Differential Input Voltage	V_{ID}	36 V	Note 2
3	Input Voltage	V_{IN}	(-Vcc-0.3V) to +Vcc	
4	Input Current (V_{IN} < - Vcc - 0.3V)	I_I	±50 mA	Note 3
5	Thermal Resistance: Junction – Ambient Junction - Case	θ_{JA} θ_{JC}	115 °C/W 28 °C/W	
6	Power Dissipation	P_D	670 mW	Note 4, 5
7	Output Short- Circuit to GND	-	Continuous	Note 6
8	Operating Temperature Range	T_A	-55 °C to +125 °C	
9	Storage Temperature Range	T_A	- 65 °C to + 150 °C	
10	Maximum Junction Temperature	Tj	150 °C	
11	Lead Temperature (Soldering, 10 s)	Tsol	300 °C	
12	Sink current	Isink	20 mA	
13	ESD Rating		600 V	Note 7

Notes:

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
2. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than -0.3 V or 0.3 V below the magnitude of negative power supply, if used (at 25 ºC).
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the Vcc voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than -0.3 V (at 25 ºC).
4. The low bias dissipation and the ON-OFF characteristics of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.
5. The maximum power dissipation must be derated at elevated temperatures and is dictate by T_{jmax} (Maximum Junction Temperature) θ_{JA} (Package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax}=(T_{jmax}-T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.
6. Short circuits from the output to Vcc can cause excessive heating and eventual destruction. When considering short circuits to ground (-Vcc), the maximum output current is approximately 20 mA independent of the magnitude of Vcc
7. Human body model, 1.5 kΩ in series with 100 pF.

Electrical DC characteristics within operating temperature range

Notes (1) (2)

Table 3

The following conditions apply, unless otherwise specified +Vcc = +5V, -Vcc = 0V, +Vin = 0V

Parameter	Symbol	Test Method MIL-STD 883	Conditions		T_A, °C	Limits Min	Limits Max	Units
Input Offset Voltage	V_{IO}	4001	$+V_{CC}$ = +30V, $-V_{CC}$ = 0V, V_L = +30V, V_T = +1.5V, R_L = 15kΩ		+22±3	-2	2	mV
					+125(+0-3)	-4	4	
					-55(+5-0)	-4	4	
				R	+22±3	-4	4	
			$+V_{CC}$ = +1.5V, $-V_{CC}$ = -28.5V, V_L = +1.5V, V_T = -27V, R_L = 15kΩ		+22±3	-2	2	
				R	+22±3	-4	4	
			$+V_{CC}$ = +2V, $-V_{CC}$ = -28V, V_L = +2V, V_T = -26.5V, R_L = 15kΩ		+22±3	-2	2	
					+125(+0-3)	-4	4	
					-55(+5-0)	-4	4	
				R	+22±3	-4	4	
			$+V_{CC}$ = +5V, $-V_{CC}$ = 0V, V_L = +5V, V_T = +1.5V, R_L = 15kΩ		+22±3	-2	2	
					+125(+0-3)	-4	4	
					-55(+5-0)	-4	4	
				R	+22±3	-4	4	
			$+V_{CC}$ = +2V, $-V_{CC}$ = -3V, V_L = +2V, V_T = -1.5V, R_L = 15kΩ		+22±3	-2	2	
					+125(+0-3)	-4	4	
					-55(+5-0)	-4	4	
				R	+22±3	-4	4	
Input Bias Current	$\pm I_{IB}$	4001	$+V_{CC}$ = 30V, $-V_{CC}$ = 0V, V_L = +30V, V_T = +1.5V, R_L = 15kΩ		+22±3	-100	1	nA
					+125(+0-3)	-300	10	
					-55(+5-0)	-300	1	
				R	+22±3	-110	1	
			$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_L = +2V, V_T = -26.5V, R_L = 15kΩ		+22±3	-100	1	
					+125(+0-3)	-300	10	
					-55(+5-0)	-300	1	
				R	+22±3	-110	1	
			$+V_{CC}$ = +5V, $-V_{CC}$ = 0V, V_L = +5V, V_T = +1.5V, R_L = 15kΩ		+22±3	-100	1	
					+125(+0-3)	-300	10	
					-55(+5-0)	-300	1	
				R	+22±3	-110	1	
			$+V_{CC}$ = +2V, $-V_{CC}$ = -3V, V_L = +2V, V_T = -1.5V, R_L = 15kΩ		+22±3	-100	1	
					+125(+0-3)	-300	10	
					-55(+5-0)	-300	1	
				R	+22±3	-110	1	

Electrical DC characteristics within operating temperature range Notes (1) (2)

The following conditions apply, unless otherwise specified +Vcc = +5V, -Vcc = 0V, +Vin = 0V

Table 3 (Continued)

Parameter	Symbol	Test Method MIL-STD 883	Conditions		T_A, °C	Limits		Units
						Min	Max	
Input Offset Current	I_{IO}	4001	$+V_{CC}$ = +30V, $-V_{CC}$ = 0V, V_L = +30V, V_T = +1.5V, R_L = 15kΩ		+22±3	-25	25	nA
					+125(+0-3)	-100	100	
					-55(+5-0)	-100	100	
				R	+22±3	-111	111	
			$+V_{CC}$ = +2V, $-V_{CC}$ = -28V, V_L = +2V, V_T = -26.5V, R_L = 15kΩ		+22±3	-25	25	
					+125(+0-3)	-100	100	
					-55(+5-0)	-100	100	
				R	+22±3	-111	111	
			$+V_{CC}$ = +5V, $-V_{CC}$ = 0V, V_L = +5V, V_T = +1.5V, R_L = 15kΩ		+22±3	-25	25	
					+125(+0-3)	-100	100	
					-55(+5-0)	-100	100	
				R	+22±3	-111	111	
			$+V_{CC}$ = +2V, $-V_{CC}$ = -3V, V_L = +2V, V_T = -1.5V, R_L = 15kΩ		+22±3	-25	25	
					+125(+0-3)	-100	100	
					-55(+5-0)	-100	100	
				R	+22±3	-111	111	
Power Supply Current	I_{CC}	4005	$+V_{CC}$ = 30V, $-V_{CC}$ = 0V, Vin_+ = +1.0V, Vin- = 0V, R_L = ∞		+22±3	-	2	mA
					+125(+0-3)			
					-55(+5-0)			
			$+V_{CC}$ = 36V, $-V_{CC}$ = 0V, Vin_+ = +1.0V, Vin- = 0V, R_L = ∞		+22±3	-	2	
					+125(+0-3)			
					-55(+5-0)			
			$+V_{CC}$ = 5V, $-V_{CC}$ = 0V, Vin_+ = +1.0V, Vin- = 0V, R_L = ∞		+22±3	-	2	
					+125(+0-3)			
					-55(+5-0)			
Voltage Gain	A_V	4004	$+V_{CC}$ = +15V, $-V_{CC}$ = 0V, V_L = +15V, V_{T1} = +1V, V_{T2} = +11V, R_L = 15kΩ		+22±3	50	-	V/mV
					+125(+0-3)	25	-	
					-55(+5-0)	25	-	
Output Sink Current	Isink	3011	+Vcc = +5V, -Vcc = 0V, Vo = 1.5V, Vin_+ = 0V, Vin- = +1V		+22±3	6	-	mA
Common Mode Rejection Ratio	CMRR	4003	Measurement V_{01}: $+V_{CC}$ = +5V, $-V_{CC}$ = 0V, V_L = +5V, V_T = +1.5V, R_L = 15kΩ Measurement V_{02}: $+V_{CC}$ = +2V, $-V_{CC}$ = -3V, V_L = +2V, V_T = -1.5V, R_L = 15kΩ		+22±3	70	-	dB
					+125(+0-3)	60	-	
					-55(+5-0)			
			Measurement V_{03}: $+V_{CC1}$= +30V, $-V_{CC}$ = 0V, V_L = +30V, V_T = +15V, R_L = 15kΩ Measurement V_{04}: $+V_{CC}$ = +1.5V, $-V_{CC}$ = -28.5V, V_L = +1.5V, V_T = -13.5V, R_L = 15kΩ		+22±3	70	-	
			Measurement V_{03}: $+V_{CC}$ = +30V, $-V_{CC}$ = 0V, V_L = +30V, V_T = +15V, R_L = 15kΩ Measurement V_{04}: $+V_{CC}$ = +2V, $-V_{CC}$ = -28V, V_L = +2V, V_T = -13V, R_L = 15kΩ		+125(+0-3)	60	-	
					-55(+5-0)			

Electrical DC characteristics within operating temperature range **Notes (1) (2)**

The following conditions apply, unless otherwise specified +Vcc = +5V, -Vcc = 0V, +Vin = 0V

Table 3 (Continued)

Parameter	Symbol	Test Method MIL-STD 883	Conditions	T_A, °C	Limits		Units
					Min	Max	
Power Supply Rejection Ratio	PSRR	4003	Measurement V_{03}: $+V_{CC}$ = +30V, $-V_{CC}$ = 0V, V_L = +30V, V_T = +1.5V, R_L = 15kΩ Measurement V_{04}: $+V_{CC}$ = +5V, $-V_{CC}$ = 0V, V_L = +5V, V_T = +1.5V, R_L = 15kΩ	+22±3	60	-	dB
Saturation Voltage	Vsat	3007	$+V_{CC}$ = +5V, $-V_{CC}$ = 0V, Vin_+ = 0V, Vin- = +1V, Io = 4mA	+22±3	-	400	mV
				+125(+0-3)	-	700	
				-55(+5-0)			
Output Leakage current	I_{CEX}	4001	$+V_{CC}$ = +30V, $-V_{CC}$ = 0V, V_L = +30V, Vin_+ = +1.0V, Vin_- = 0V	+22±3	-	1.0	µA
				+125(+0-3)			
				-55(+5-0)			
Common mode voltage range (note 4)	V_{CM}	4003	Measurement V_{03}: $+V_{CC}$ = +30V, $-V_{CC}$ = 0V, V_L = +30V, V_T = +15V, R_L = 15kΩ Measurement V_{04}: $+V_{CC}$ = +1.5V, $-V_{CC}$ = -28.5V, V_L = +1.5V, V_T = -13.5V, R_L = 15kΩ	+22±3	0	+Vcc -1.5	V
			Measurement V_{03}: $+V_{CC}$ = +30V, $-V_{CC}$ = 0V, V_L = +30V, V_T = +15V, R_L = 15kΩ Measurement V_{04}: $+V_{CC}$ = +2V, $-V_{CC}$ = -28V, V_L = +2V, V_T = -13V, R_L = 15kΩ	+125(+0-3)	0	+Vcc -2.0	
				-55(+5-0)			
Input Leakage Current (Differential Input Voltage) (note 5, 6)	$\pm I_{IL}$ (Vdiff)	4001	$+V_{CC}$ = +30V, $-V_{CC}$ = 0V, V_L = +30V, Vin- = 0V, Vin+ = +36V	+22±3	-	500	nA
				+125(+0-3)			
				-55(+5-0)			
			$+V_{CC}$ = +30V, $-V_{CC}$ = 0V, V_L = +30V, Vin- = +36V, Vin+ = 0V	+22±3	-	500	nA
				+125(+0-3)			
				-55(+5-0)			
			$+V_{CC}$ = +5V, $-V_{CC}$ = 0V, V_L = +5V Vin- = -0.3V, Vin+ = +30V	+22±3	-	500	nA
				+125(+0-3)			
				-55(+5-0)			
			$+V_{CC}$ = +5V, $-V_{CC}$ = 0V, V_L = +5V Vin- = +30V, Vin+ = -0.3V	+22±3	-	500	nA
				+125(+0-3)			
				-55(+5-0)			

Notes:

(1) Post irradiation limits are identical to those listed under DC and AC electrical characteristics except as listed in the line denoted "R" (correspond to 100 krads (Si)) of "Conditions" section Table 4(a). Radiation end point limits for the noted parameters are ensured only for the conditions as specified in ESCC 22900.

(2) Low dose rate testing should be performed on a wafer-by-wafer basis, per ESCC 22900 p.5.2, with no enhanced low dose rate sensitivity (ELDRS) effect.

(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so no loading change exists on the reference or input lines.

(4) The upper end of the common mode voltage range is +Vcc -1.5 V for T_A = +22±3°C or +Vcc - 2.0 V for T_A = +125(+0-3)°C and T_A = -55(+5-0)°C. Parameter V_{CM} is estimated by measuring of CMRR (FIGURE 8(f))

(5) Parameter V_{Diff} is evaluated by measuring of $\pm I_{IL}$ and the value for V_{Diff} is not data logged during Read and Record.

(6) Either or both inputs can go from –Vcc – 0.3V to +30 V dc without damage independent of the magnitude of +Vcc. This is assessed by measuring of input leakage current.

Electrical AC characteristics within operating temperature range Notes (1) (2) (3) (4)

The following conditions apply, unless otherwise specified +Vcc= +5V, -Vcc=0V

Table 4

Parameter	Symbol	Test Method MIL-STD 883	Conditions	T_A,° C	Min	Max	Units
Response Time (Low to High), notes (3) (4)	t_{RLH}	4002	Vin = 100mV, RL = 5.1KΩ, V_{OD} = 5 mV, C_L=50pF	+22 ±3	-	5.0	µs
			Vin = 100mV, RL = 5.1KΩ, V_{OD} = 50 mV, C_L=50pF			0.8	
			R			1.0	
Response Time (High to Low), notes (3) (4)	t_{RHL}	4002	Vin = 100mV, RL = 5.1KΩ, V_{OD} = 5 mV, C_L=50pF			2.5	
			Vin = 100mV, RL = 5.1KΩ, V_{OD} = 50 mV, C_L=50pF			0.8	

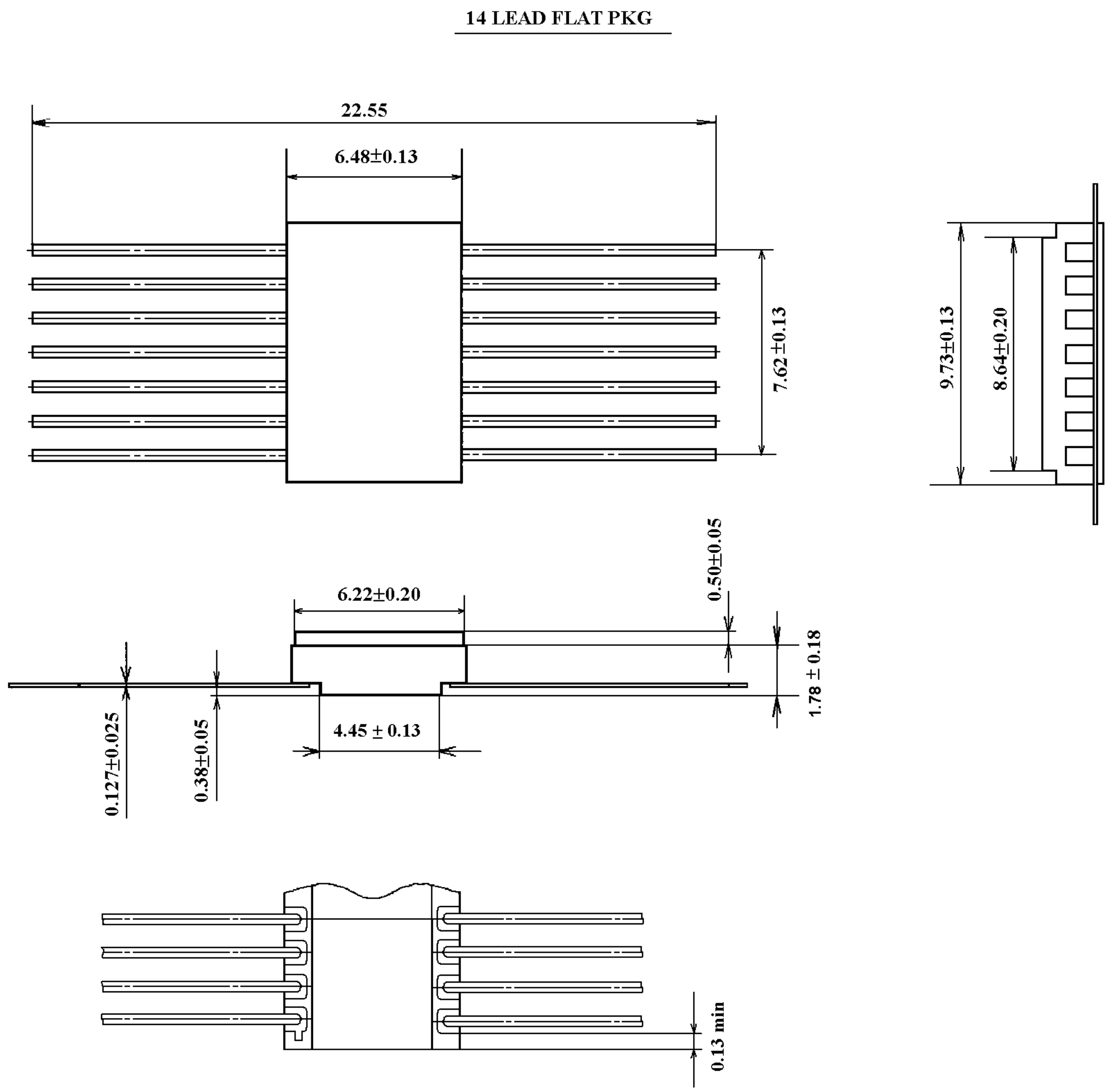
Notes:

(1) Post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the line denoted "R" (correspond to 100 krads (Si)) of "Conditions" section Table 4(b). Radiation end point limits for the noted parameters are ensured only for the conditions as specified in ESCC 22900.
(2) Low dose rate testing should be performed on a wafer-by-wafer basis, per ESCC 22900 p.5.2, with no enhanced low dose rate sensitivity (ELDRS) effect.
(3) Adjust the signal generator so that Vin is a 100mV pulse train with a 10µs pulse width at 50kHz,
Tr and Tf < 10ns and Zo = 50Ω
(4) All resistor tolerances are ±1% and all capacitor tolerances are ±10%

Physical Dimensions

Figure 3

14-lead ceramic flatpack dimensions



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